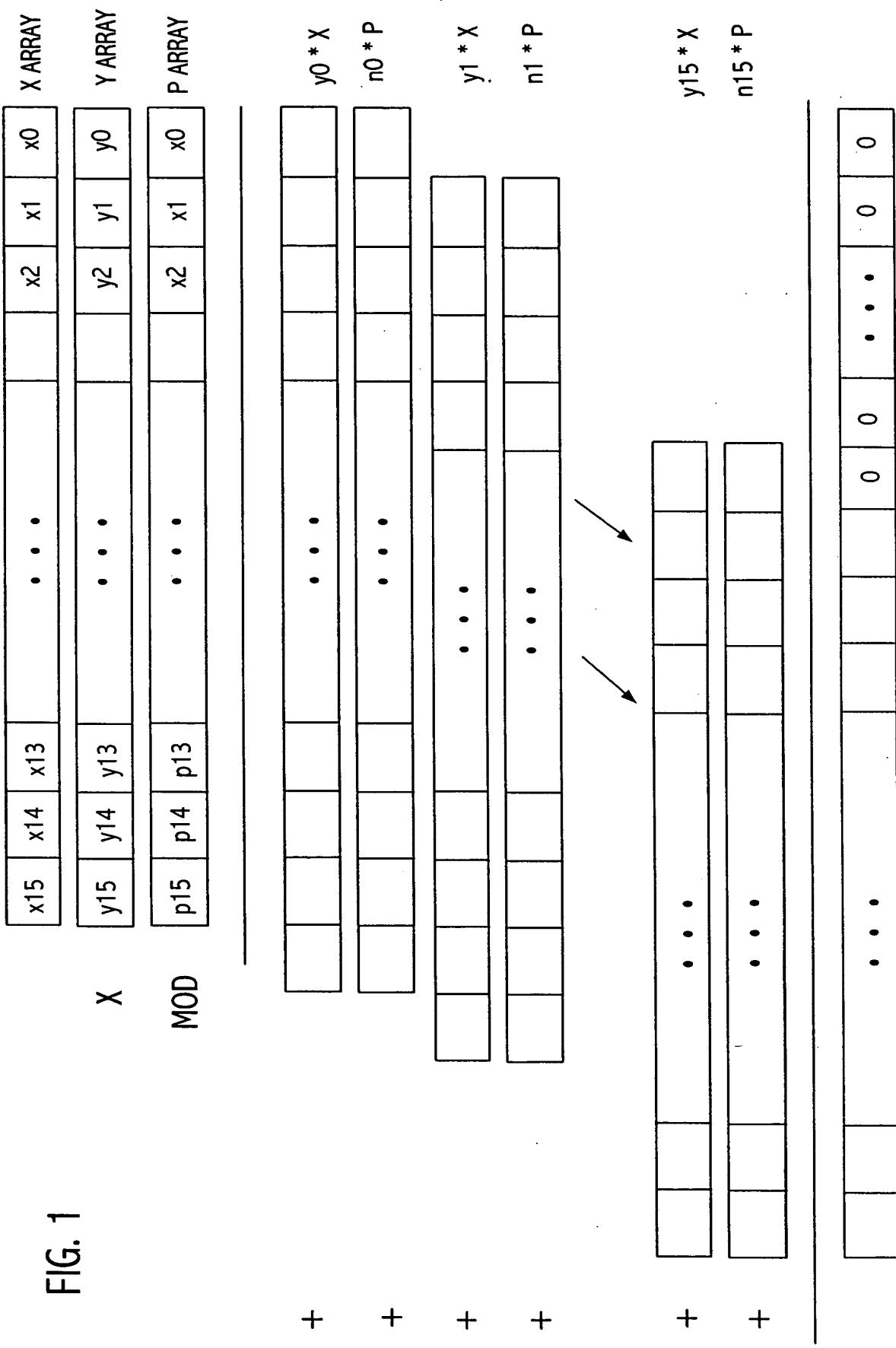


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FIG. 1



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x15	x14	x13		• • •			x2	x1	x0
+	y15	y14	y13		• • •		x2	x1	x0
<hr/>									
s16	s15	s14	s13		• • •		s2	s1	s0

FIG. 2

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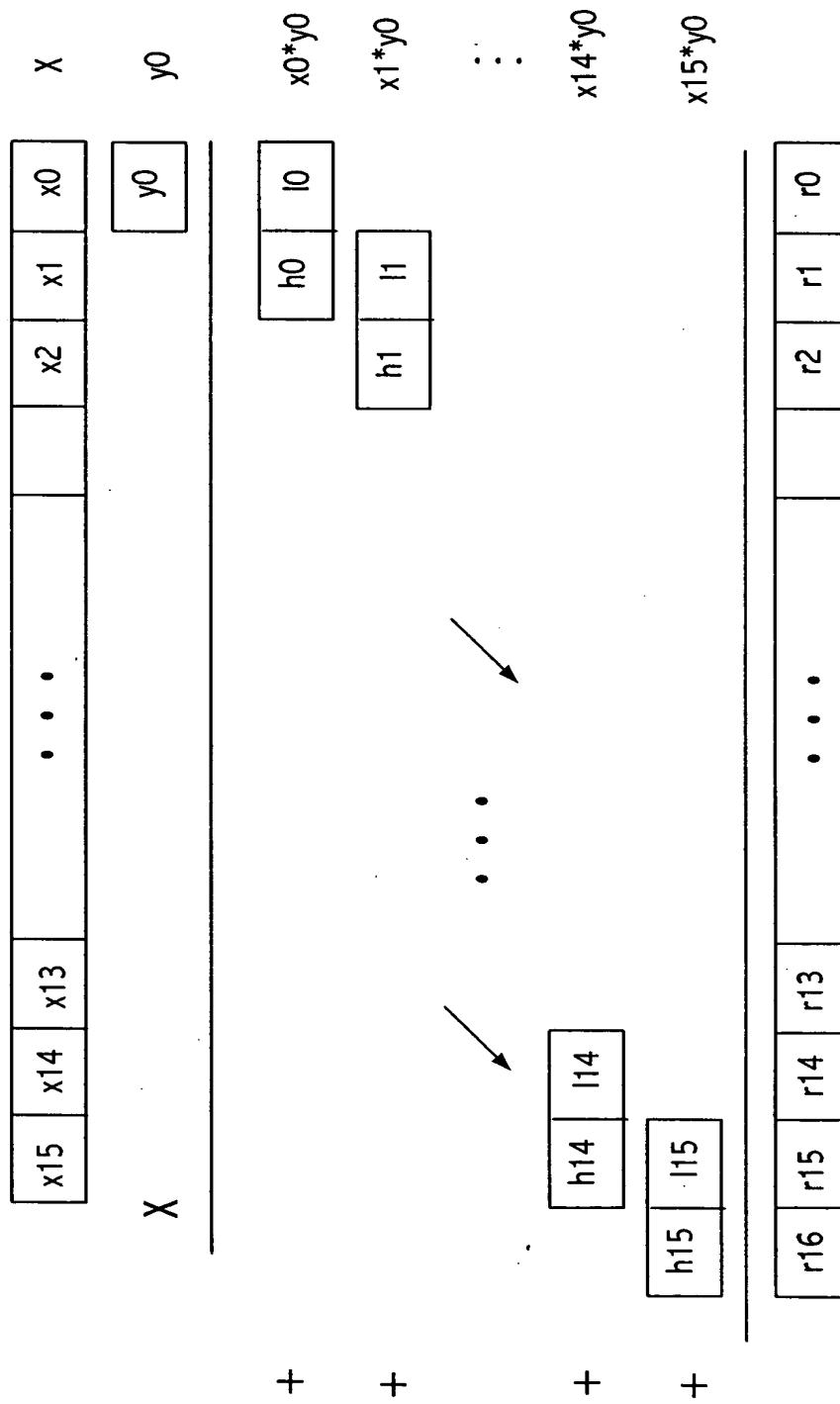


FIG. 3

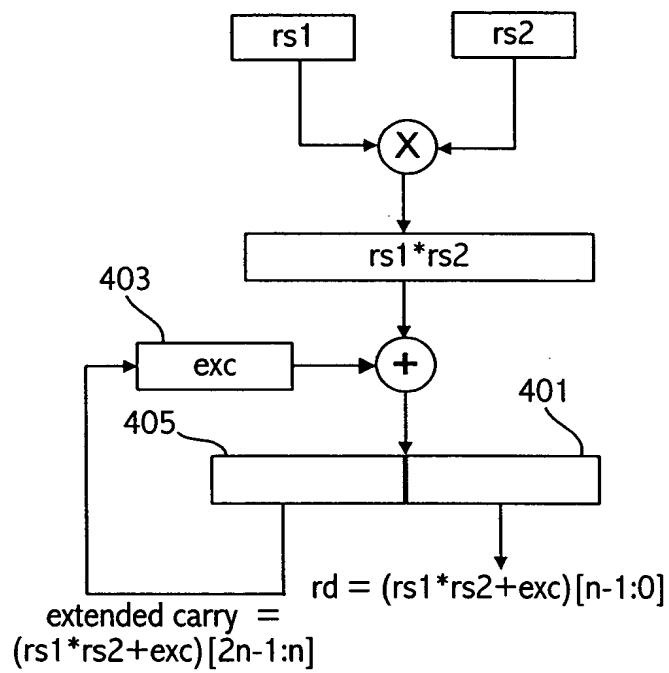


FIG. 4A

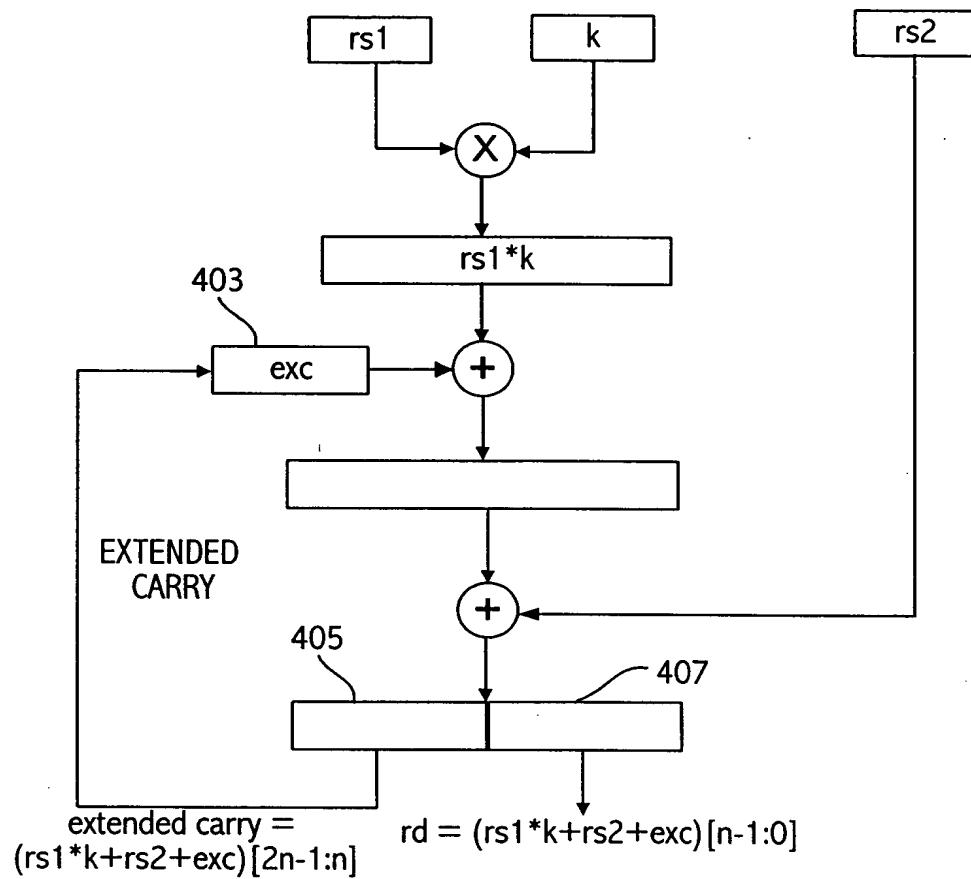


FIG. 4B

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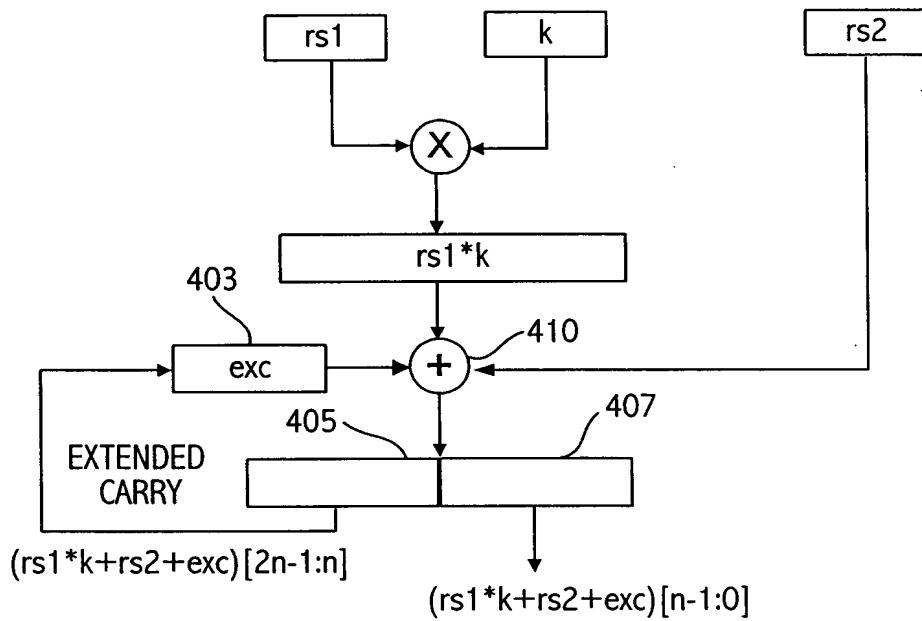


FIG. 4C

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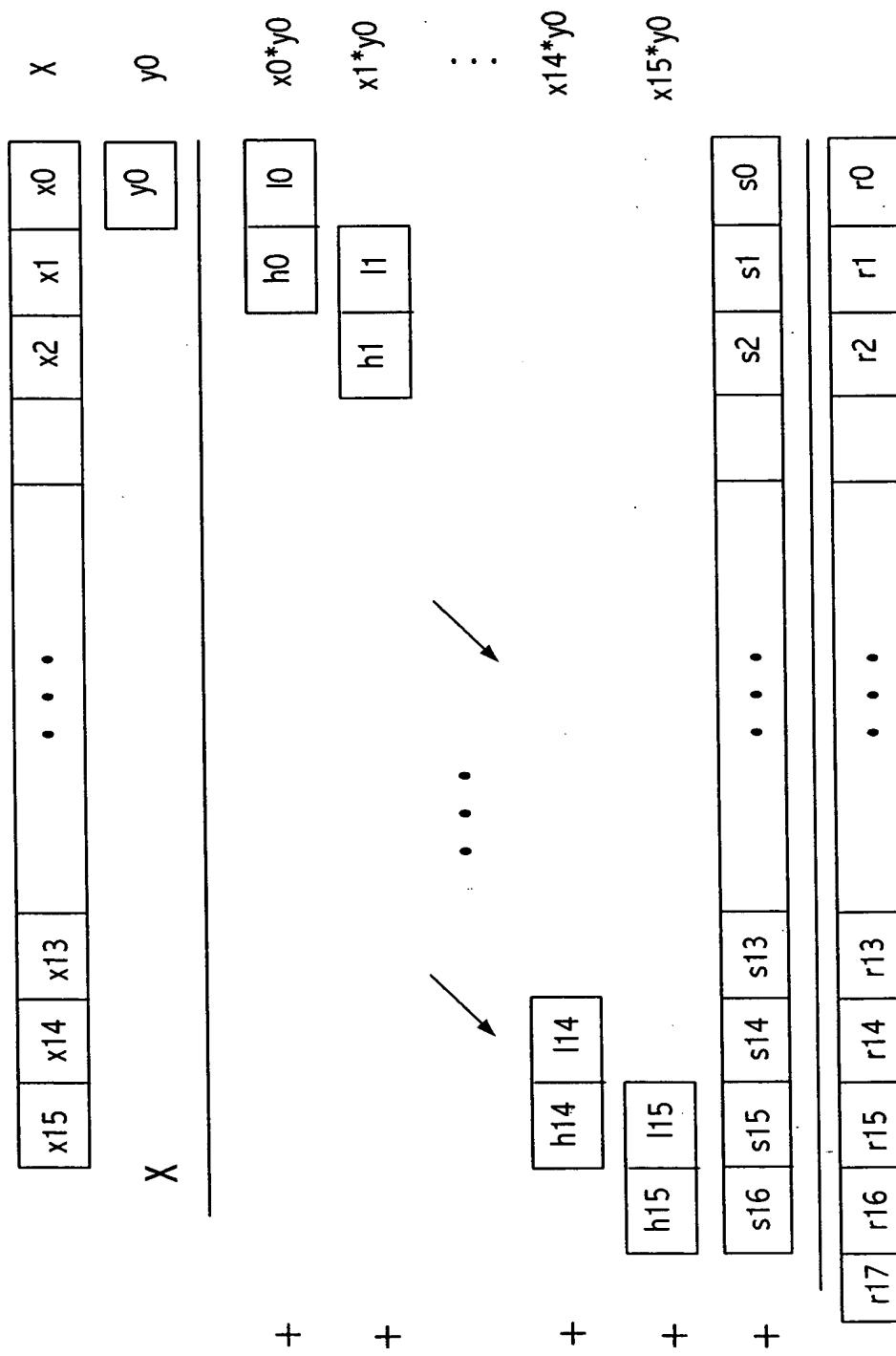


FIG. 5

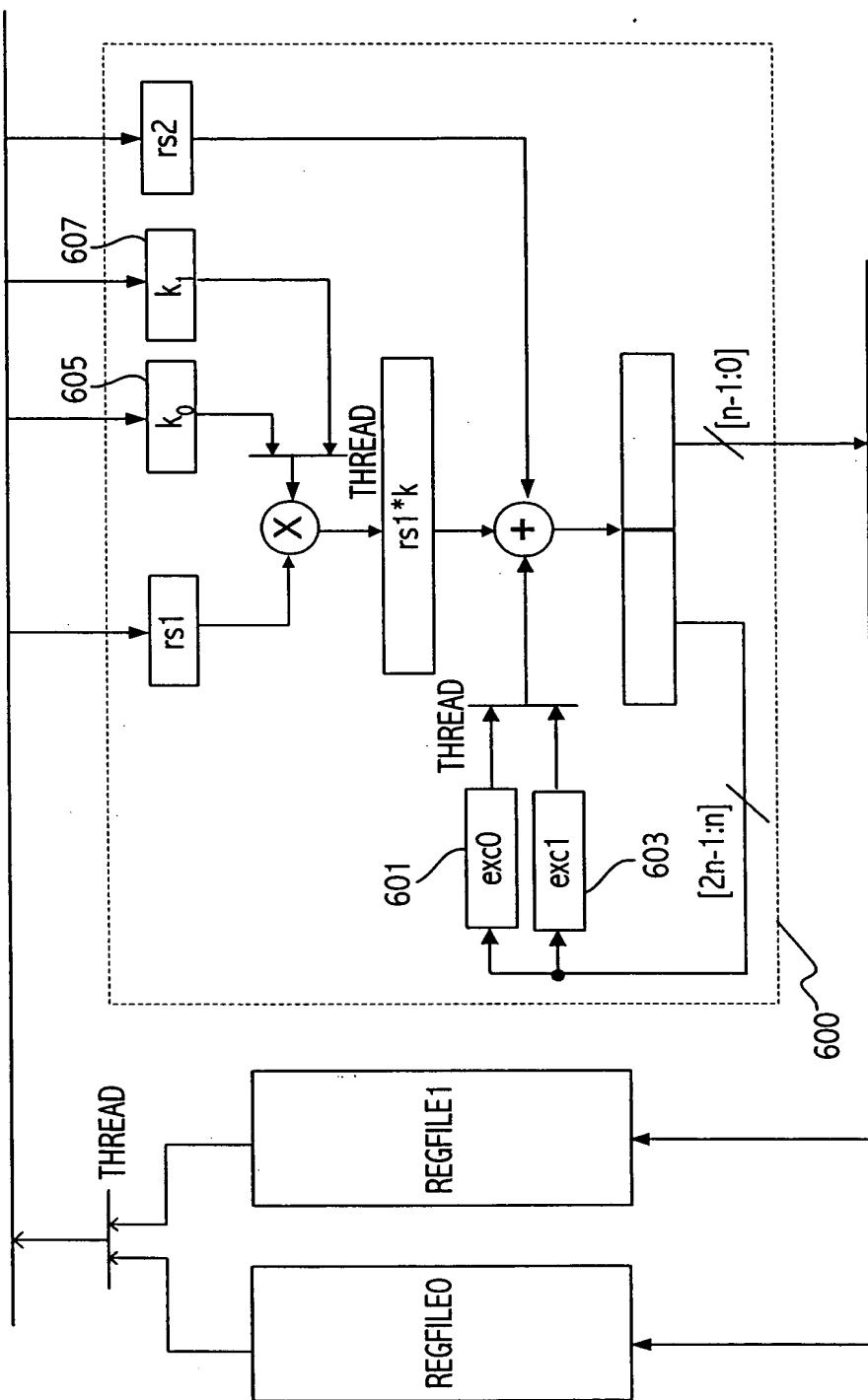


FIG. 6

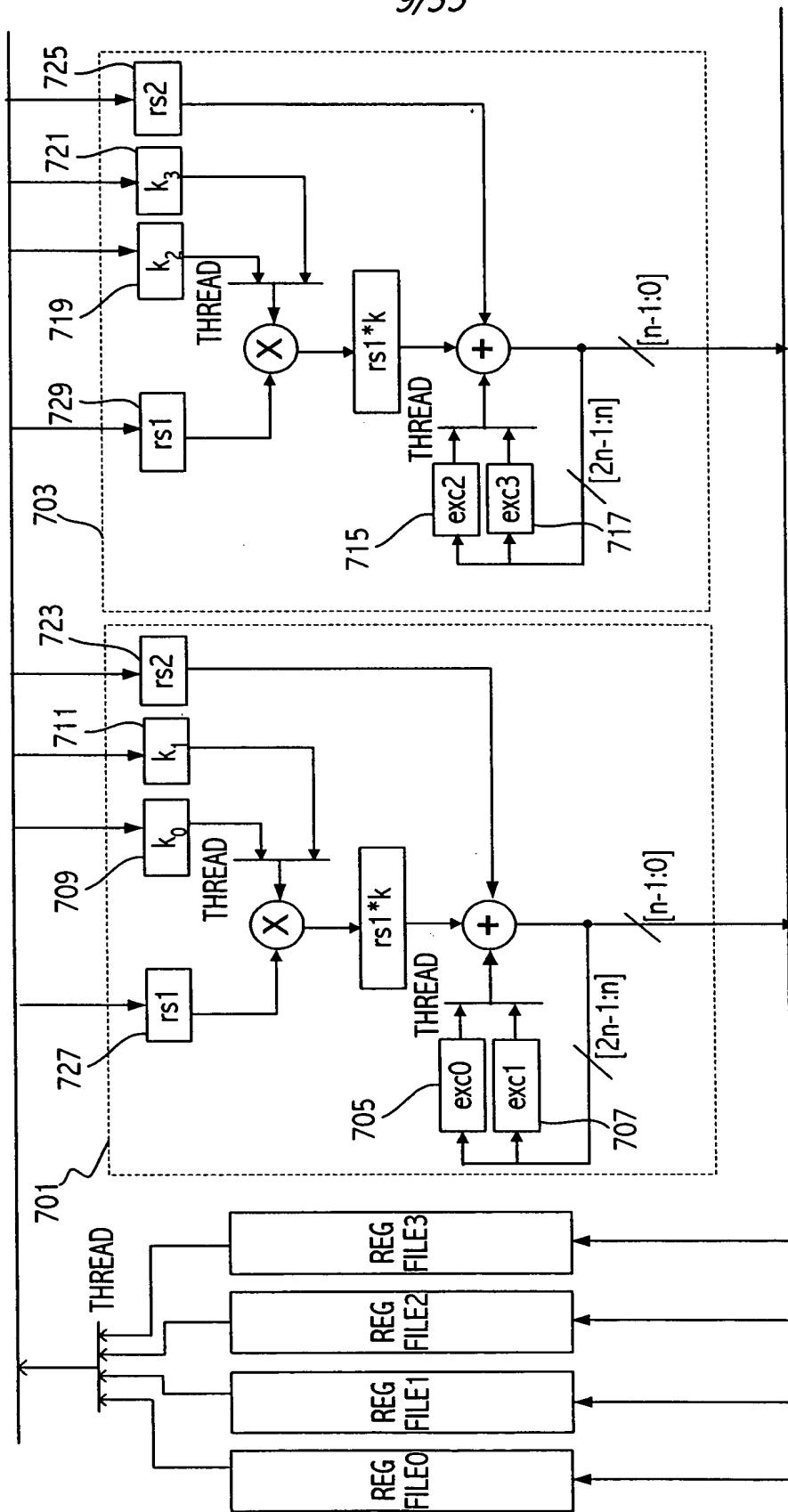


FIG 7

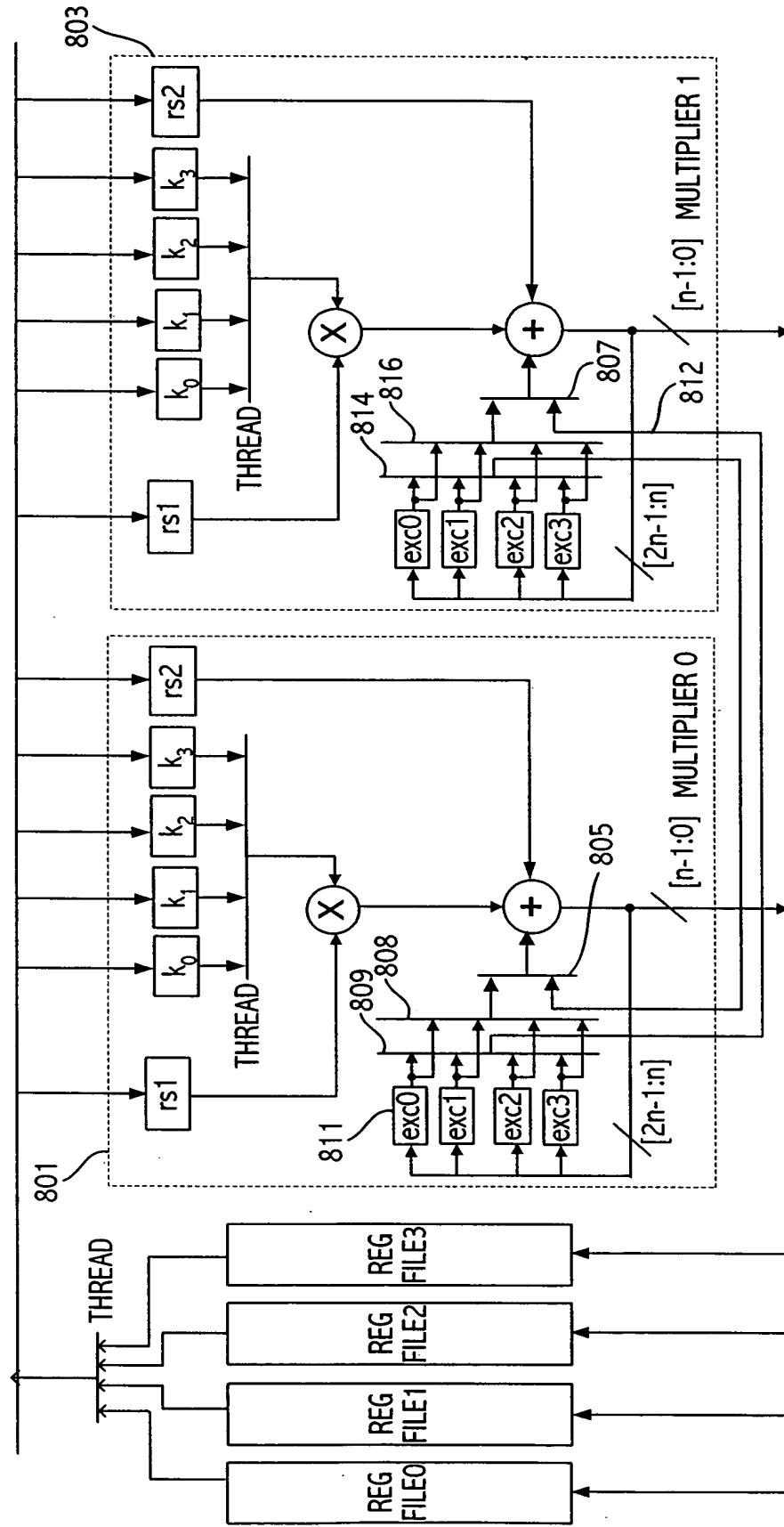


FIG. 8

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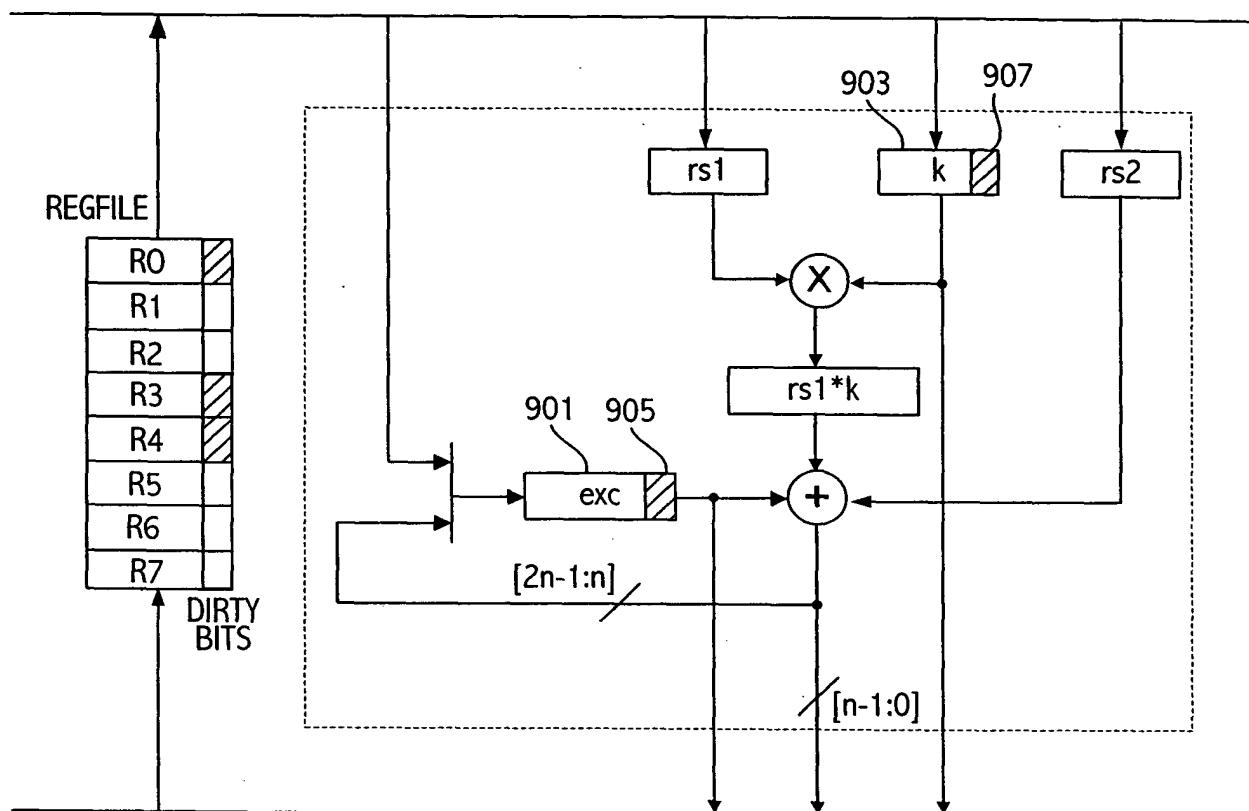


FIG. 9

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$$\begin{array}{l}
 X_3 \quad X_2 \quad X_1 \quad X_0 \quad * \quad Y_3 \quad Y_2 \quad Y_1 \quad Y_0 \quad + \quad EX3 \quad EX2 \quad EX1 \quad EX0 \\
 \qquad \qquad \qquad P03 \quad P02 \quad P01 \quad P00 \qquad \qquad \qquad P_{ij} \\
 + \qquad \qquad \qquad P13 \quad P12 \quad P11 \quad P10 \qquad \qquad \qquad = X_i * Y_j \\
 + \qquad \qquad \qquad P23 \quad P22 \quad P21 \quad P20 \\
 + \qquad \qquad \qquad P33 \quad P32 \quad P31 \quad P30 \\
 + \qquad \qquad \qquad EX3 \quad EX2 \quad EX1 \quad EX0 \\
 \hline
 = \qquad S6 \quad S5 \quad S4 \quad S3 \quad S2 \quad S1 \quad S0 \\
 + \quad C7 \quad C6 \quad C5 \quad C4 \quad C3 \quad C2 \quad C1 \\
 \hline
 \quad EX3 \quad EX2 \quad EX1 \quad EX0 \quad rd3 \quad rd2 \quad rd1 \quad rd0
 \end{array}$$

FIG. 10

$$\begin{array}{cccccccccccccccc}
 X_3 & X_2 & X_1 & X_0 & * & Y_3 & Y_2 & Y_1 & Y_0 & + & (0, S_6, S_5, S_4) & + & (C_7, C_6, C_5, C_4) & + & (0, 0, 0, C_4) \\
 & & & & & P_03 & P_02 & P_01 & P_00 & & & & & & & \\
 & & & & + & P_13 & P_12 & P_11 & P_10 & & & & & & & P_{ij} = X_i * Y_j \\
 & & & & + & P_23 & P_22 & P_21 & P_20 & & & & & & & \\
 & & & & + & P_33 & P_32 & P_31 & P_30 & & & & & & & \\
 & & & & + & & S_6 & S_5 & S_4 & \leftarrow & \text{PREVIOUS SUM OUTPUT} & & & & & \text{INPUTS IN MIDDLE} \\
 & & & & + & C_7 & C_6 & C_5 & C_4 & \leftarrow & \text{PREVIOUS CARRY OUTPUT} & & & & & \text{OF WALLACE TREE} \\
 & = & \hline & & S_6 & S_5 & S_4 & S_3 & S_2 & S_1 & S_0 & \} & \text{NEW WALLACE TREE SUM OUTPUT} \\
 & & & + & C_7 & C_6 & C_5 & C_4 & C_3 & C_2 & C_1 & \} & \text{NEW WALLACE TREE CARRY OUTPUT}
 \end{array}$$

FIG. 11

$$\begin{array}{r}
 & S3 & S2 & S1 & S0 \\
 + & C3 & C2 & C1 & \\
 + & & & CC4 & \xleftarrow{\text{← PREVIOUS CLA CARRY OUT}} \\
 \hline
 CC4 & RD3 & RD2 & RD1 & RDO \xleftarrow{\text{← NEW CLA OUTPUT}}
 \end{array}$$

FIG. 12

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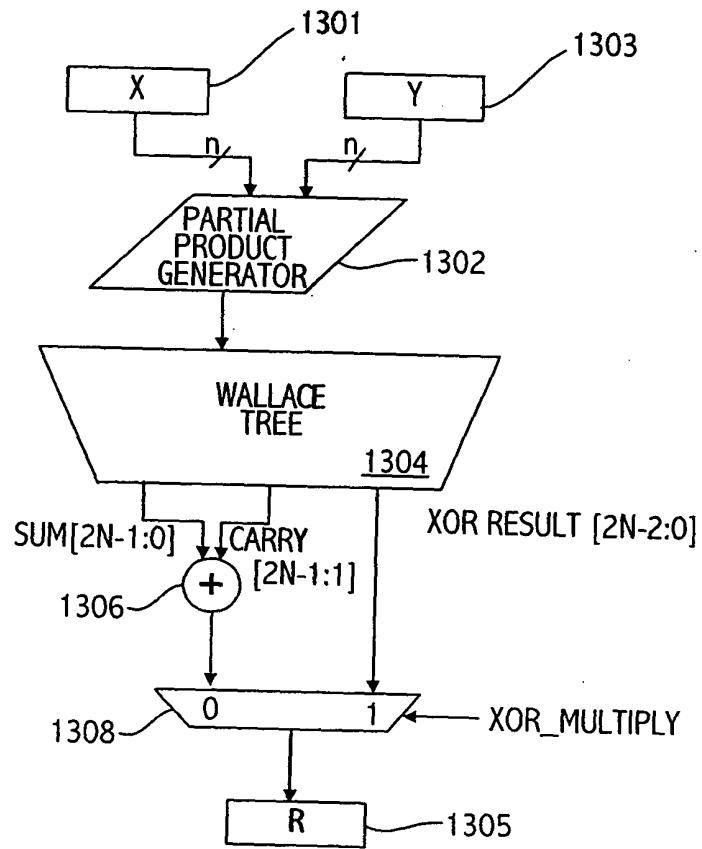


FIG. 13

with $[S7:S0]$ and $[C7:C0]$ going to the carry look-ahead adder.

Fig 12 B

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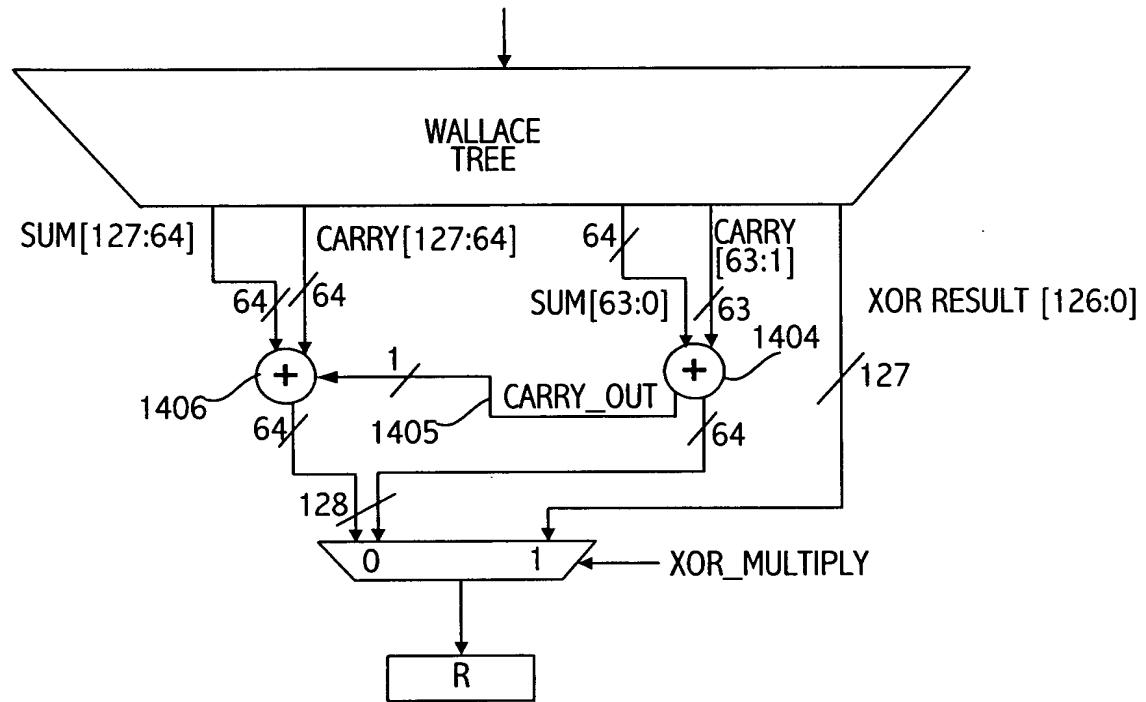


FIG. 14

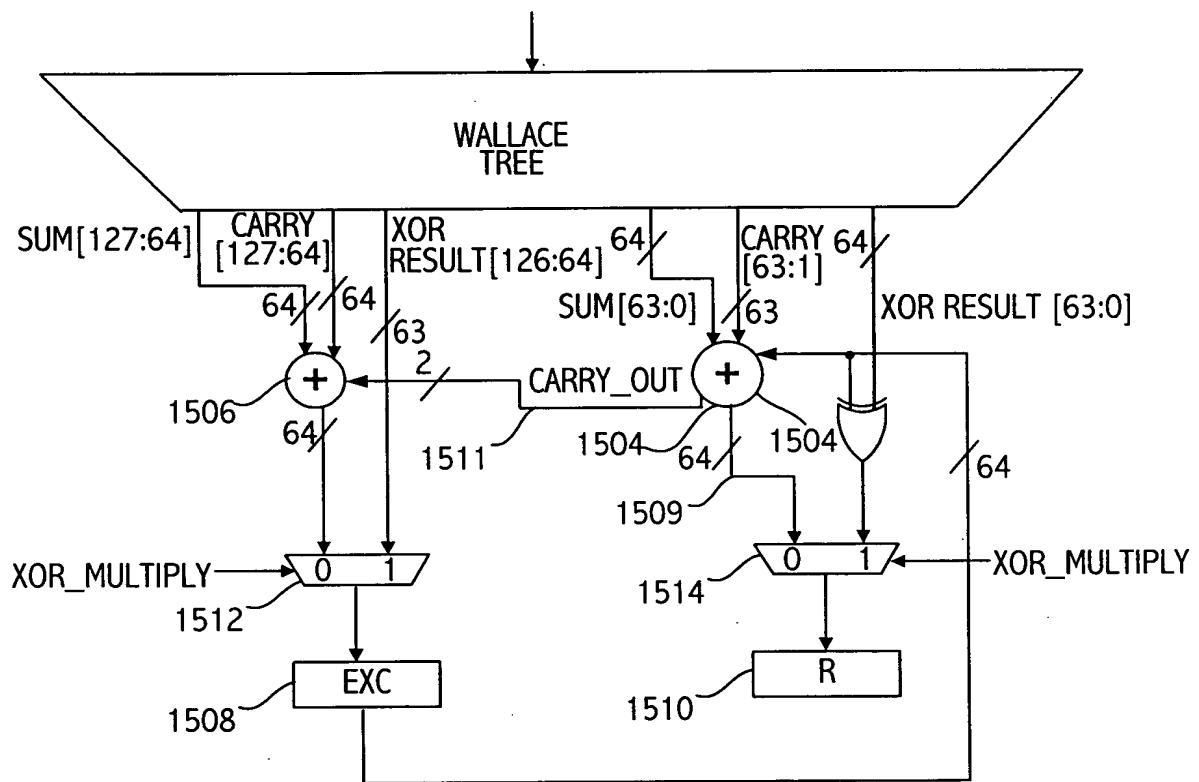


FIG. 15

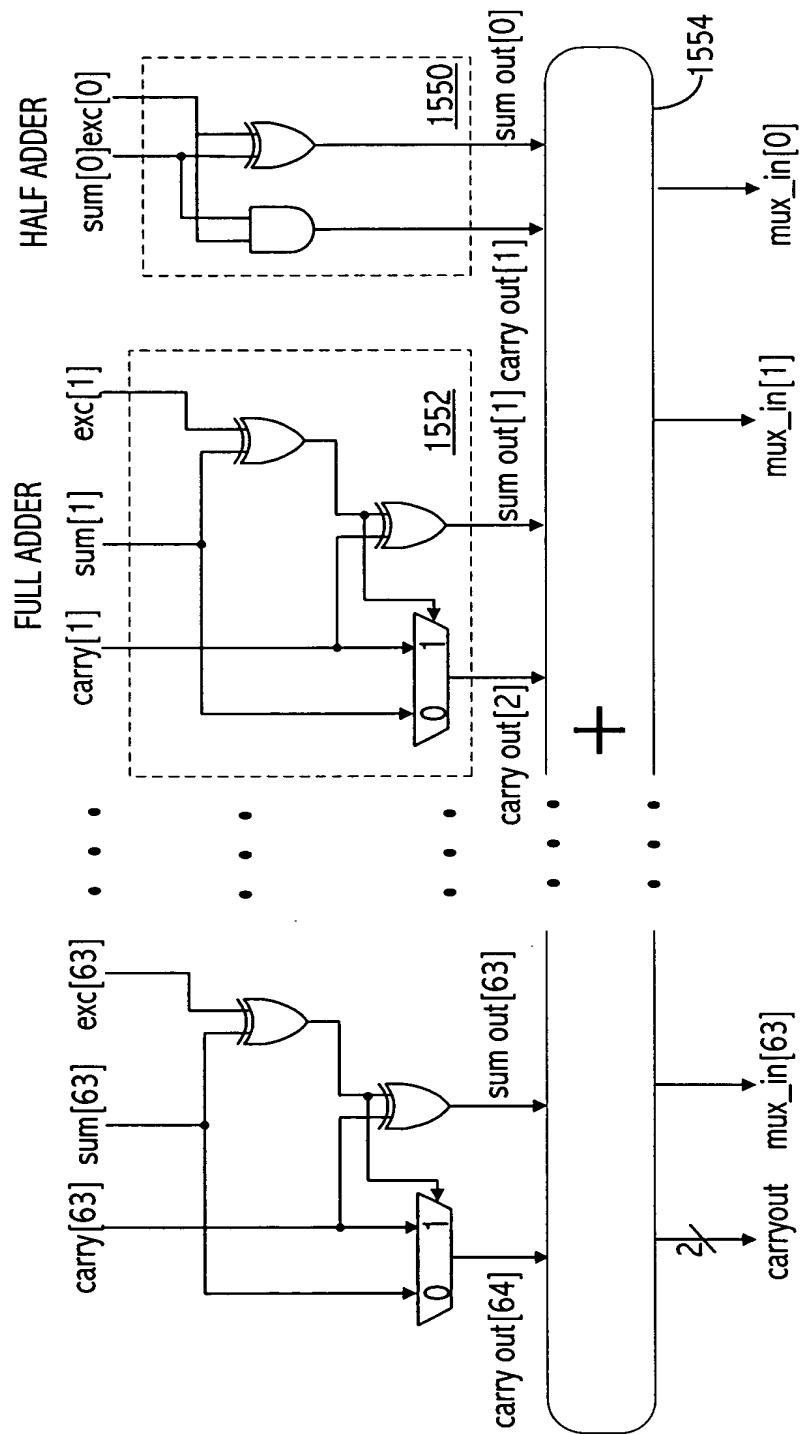


FIG. 15a

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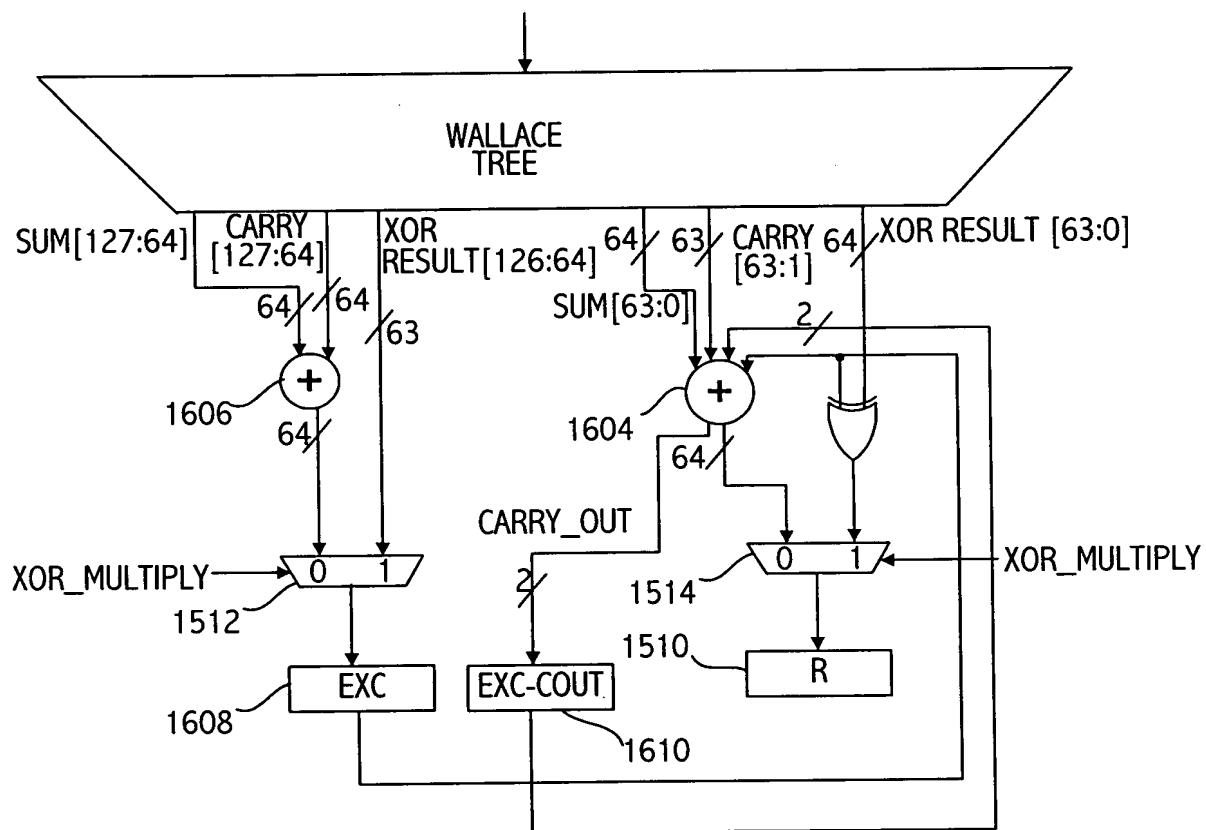


FIG. 16

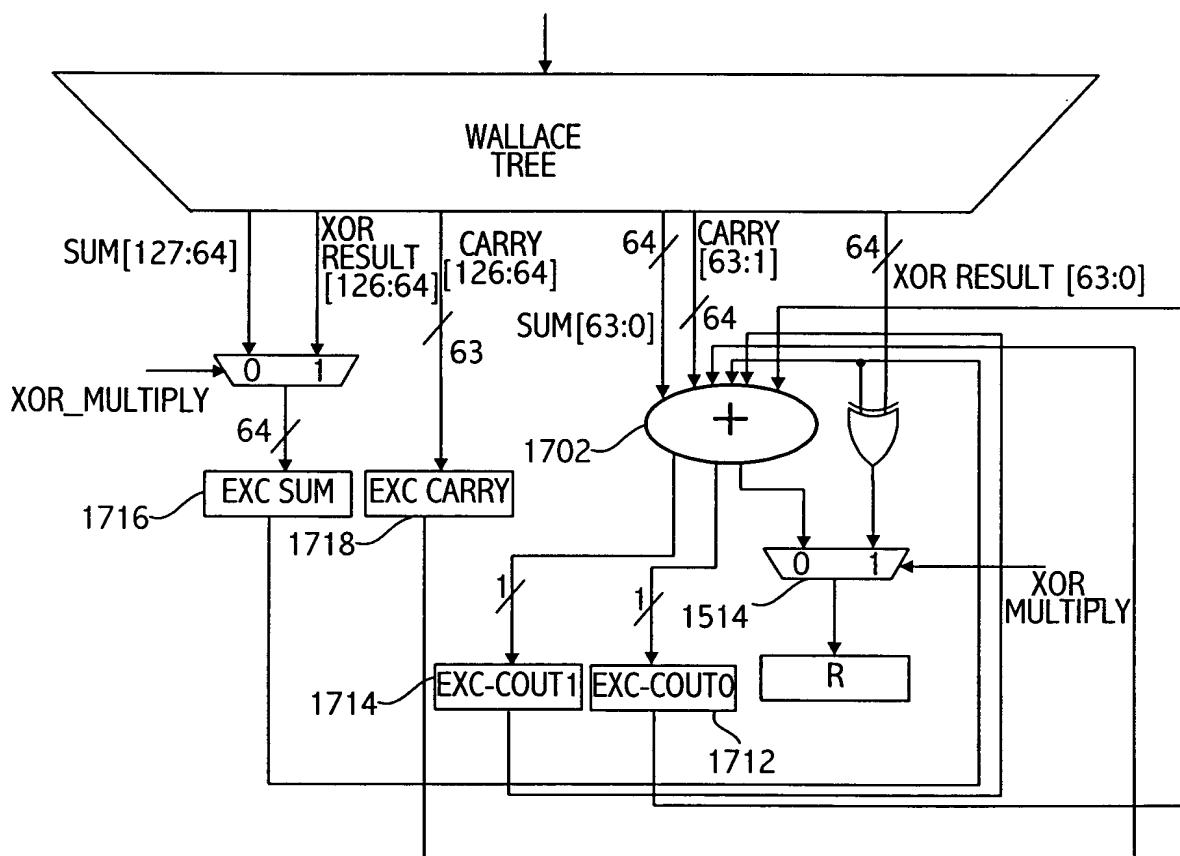


FIG. 17

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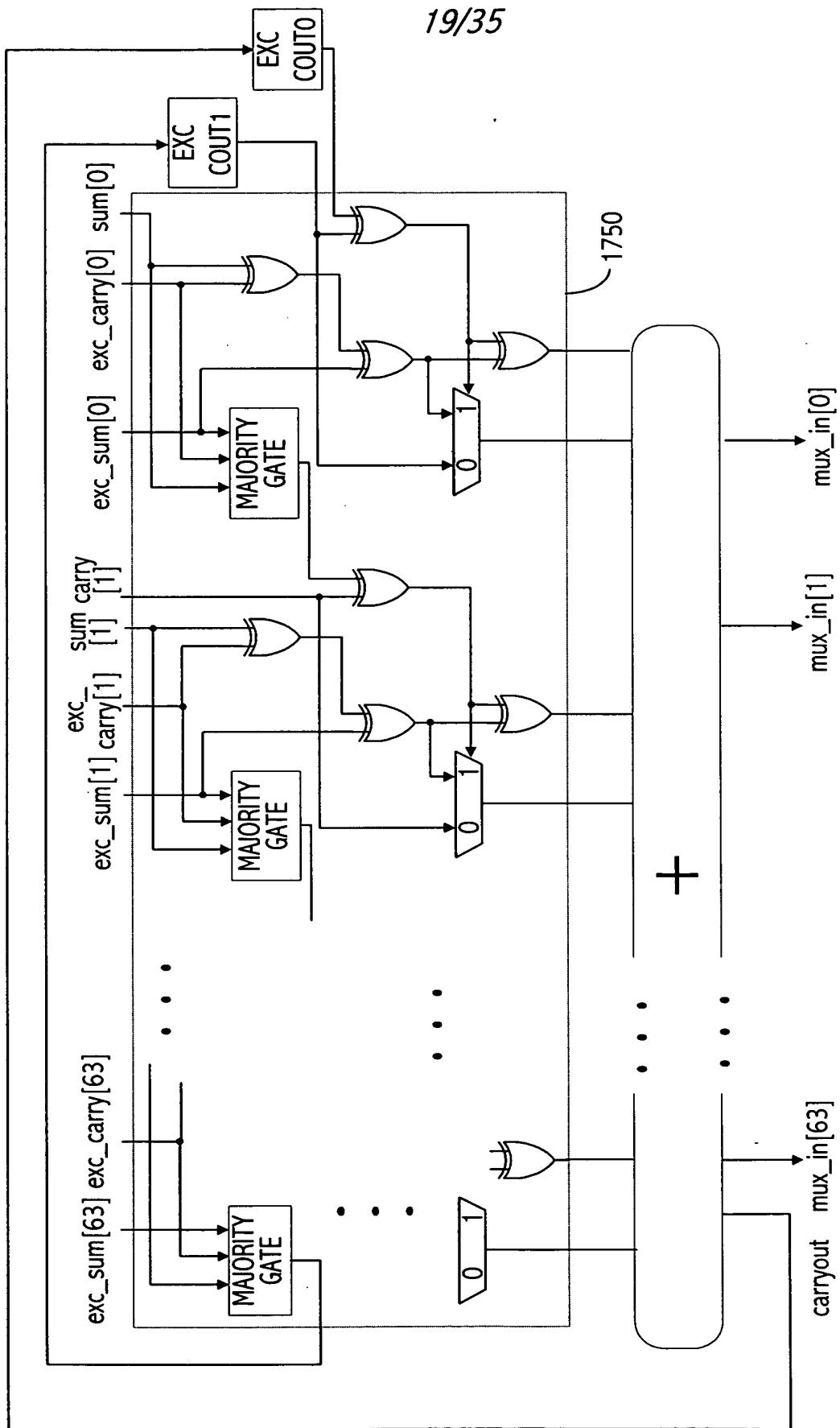


Fig. 17A

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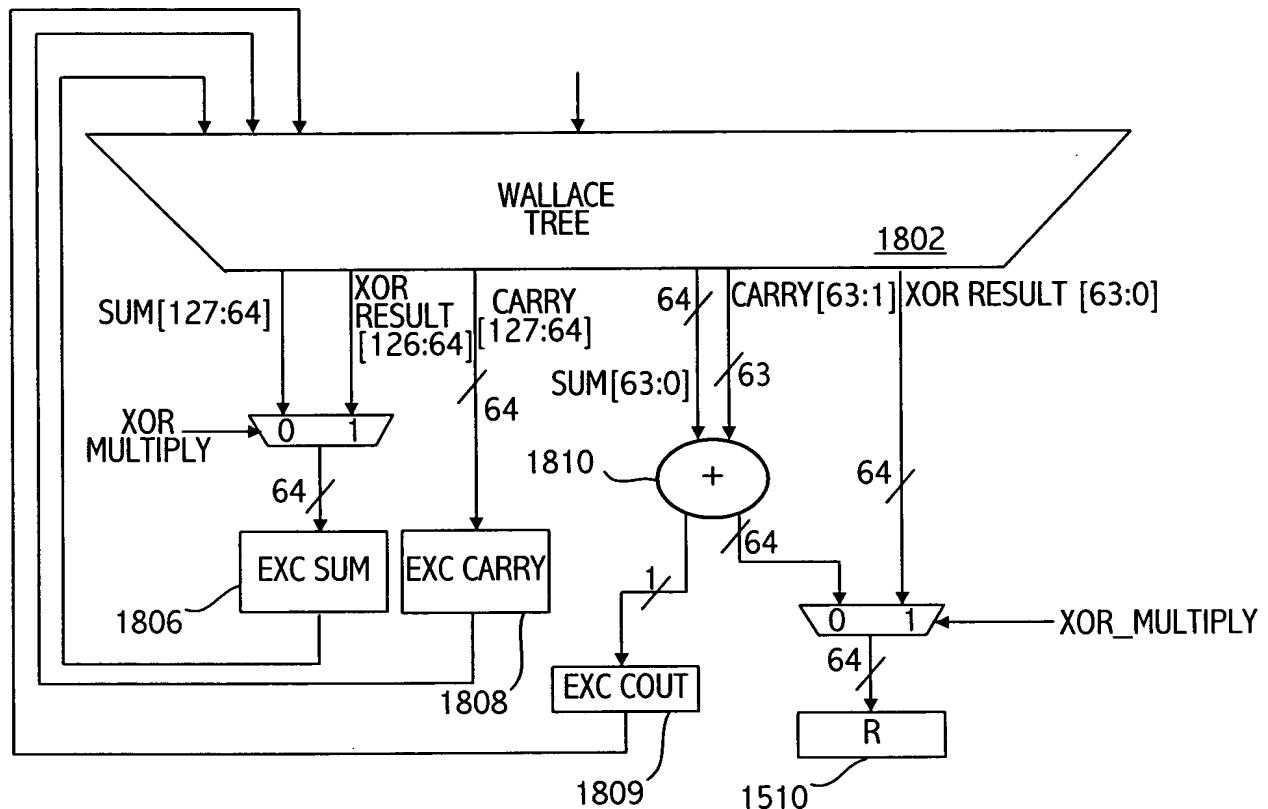


FIG. 18

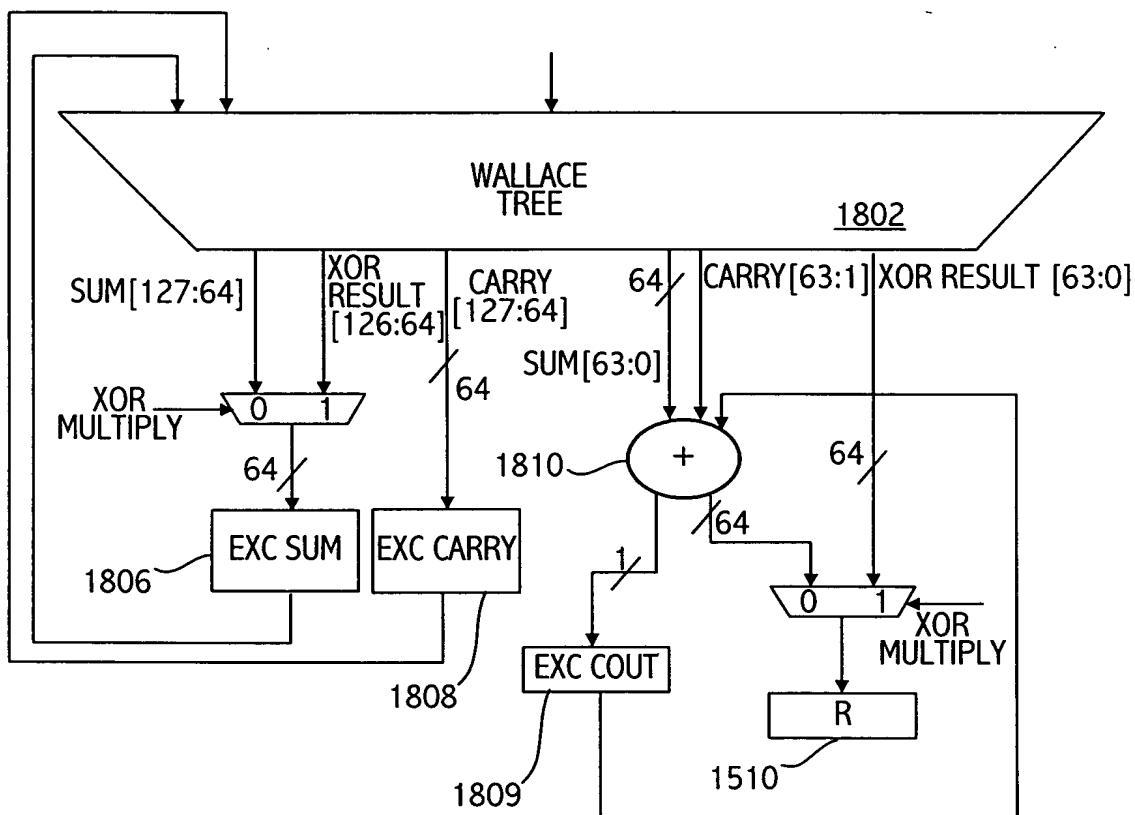


FIG. 19

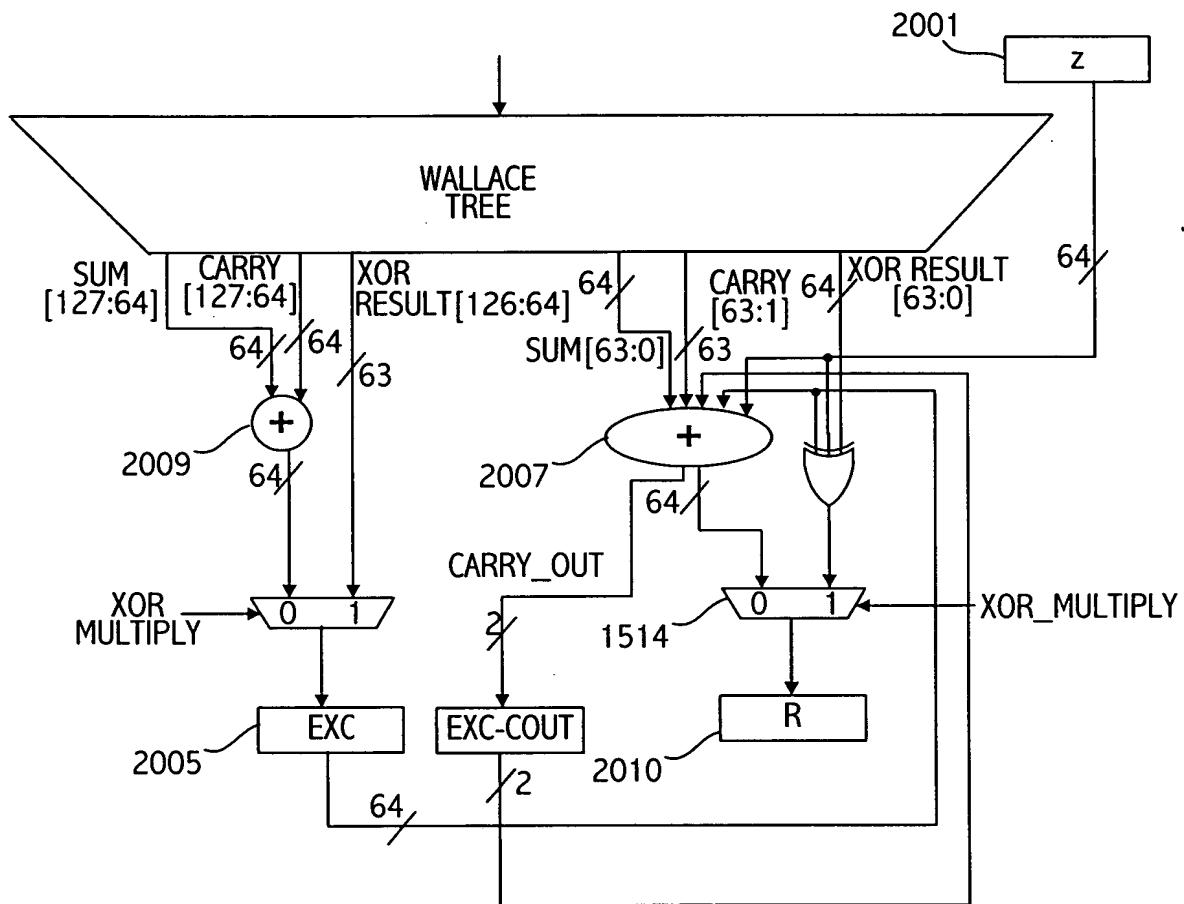


FIG. 20

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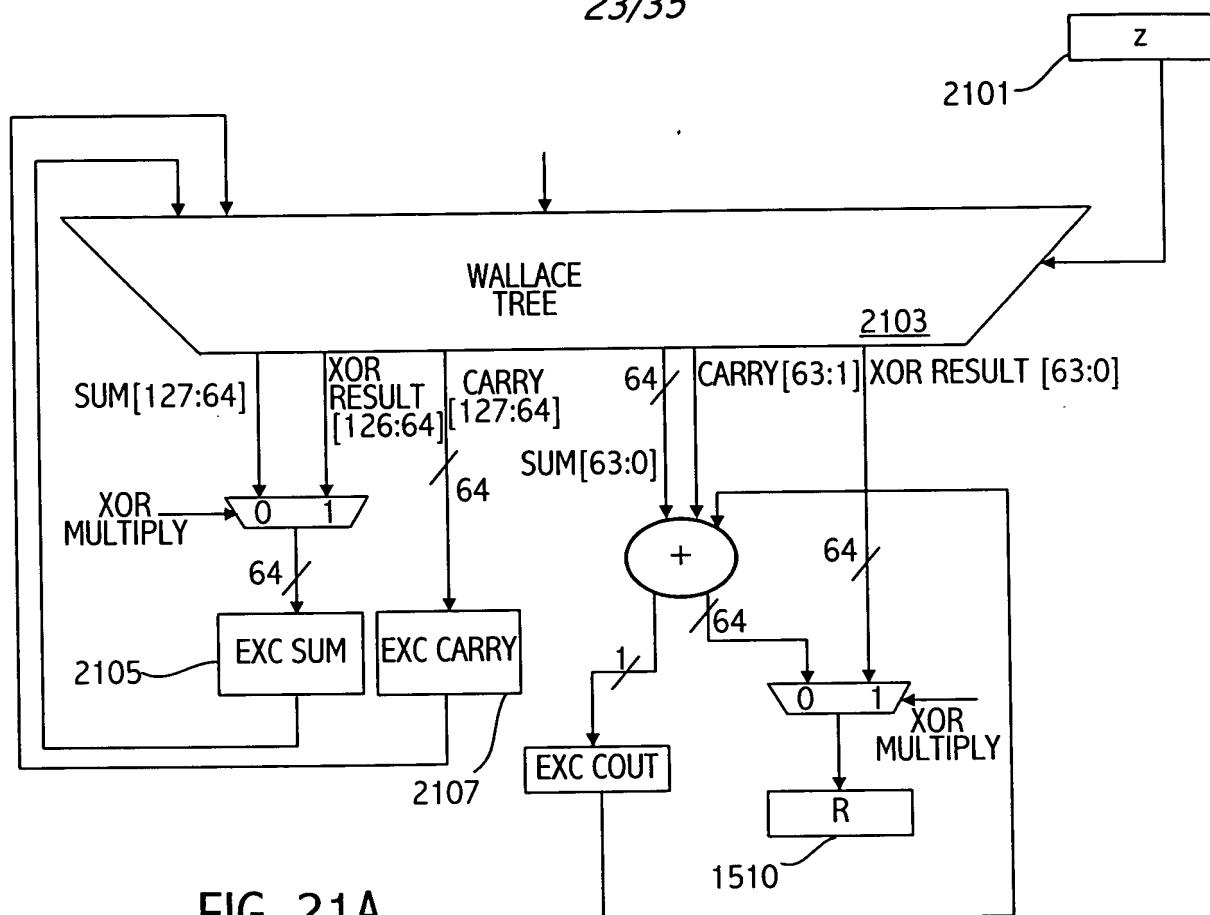


FIG. 21A

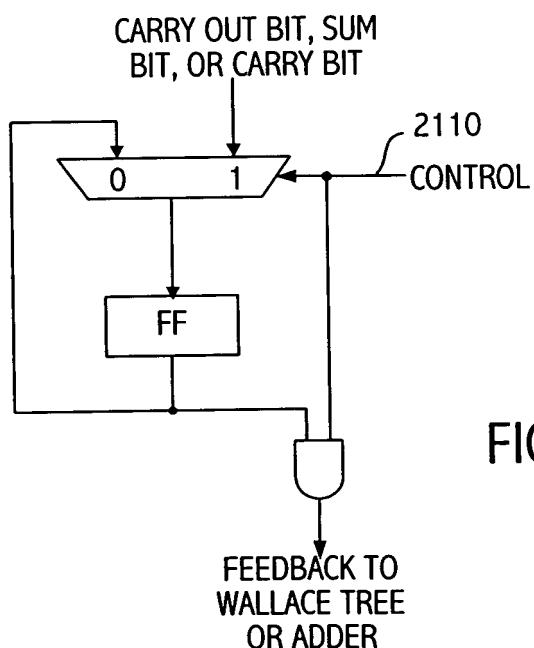


FIG. 21B

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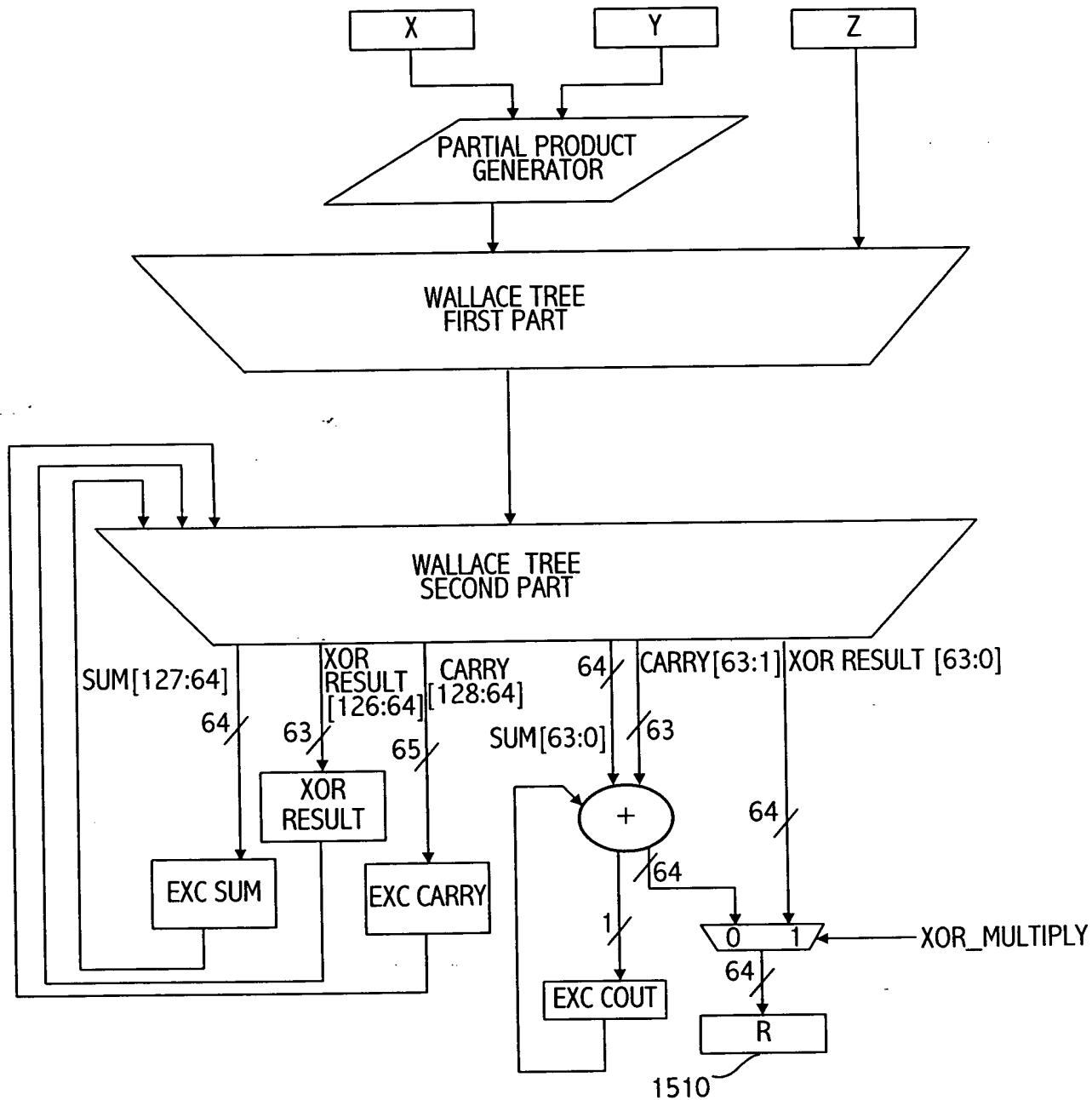


FIG. 21C

XOR

MUX

MAJORITY

**MUL
MAJORITY**

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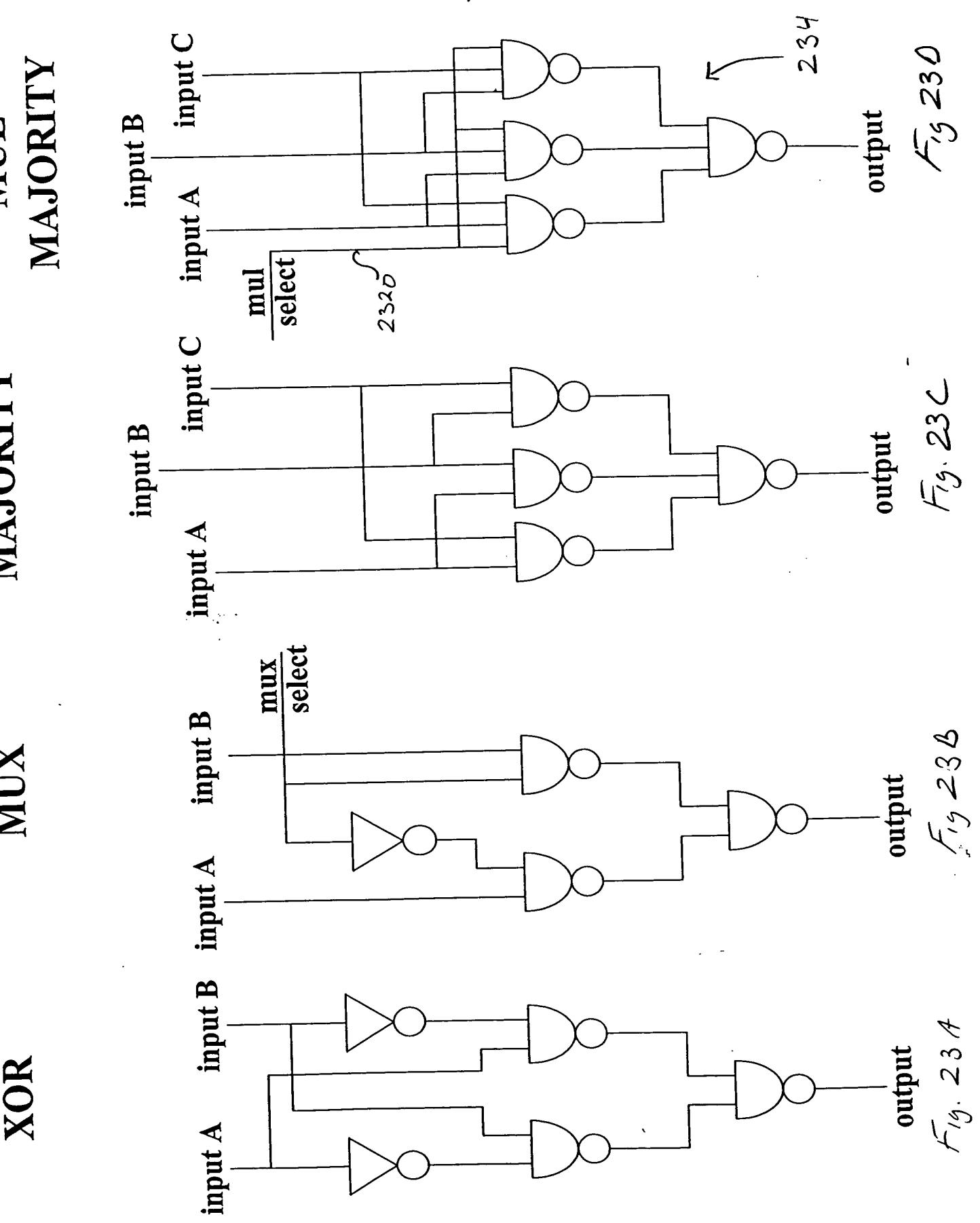


Fig. 23A

Fig. 23B

Fig. 23C

Fig. 23D

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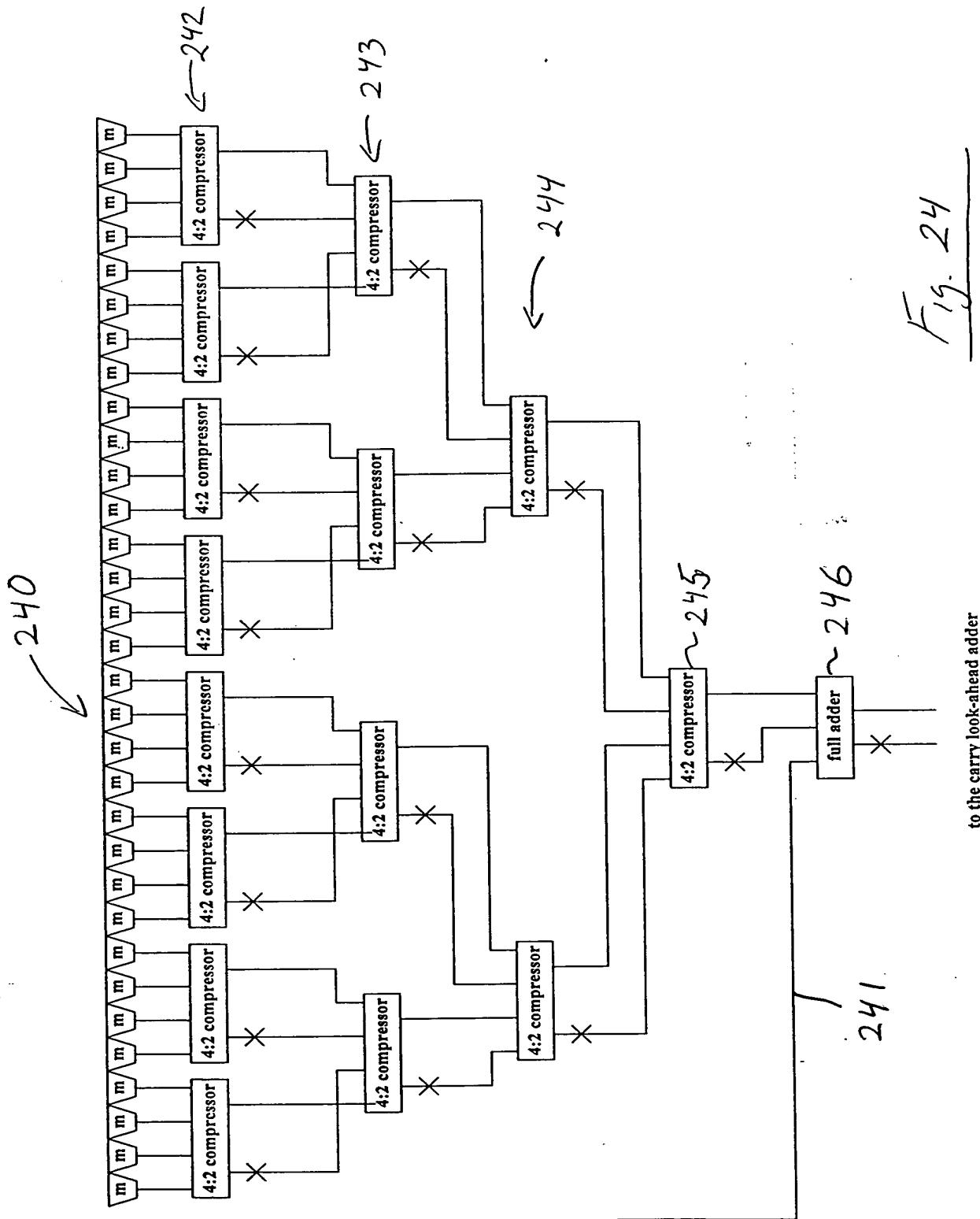


Fig. 24

to the carry look-ahead adder

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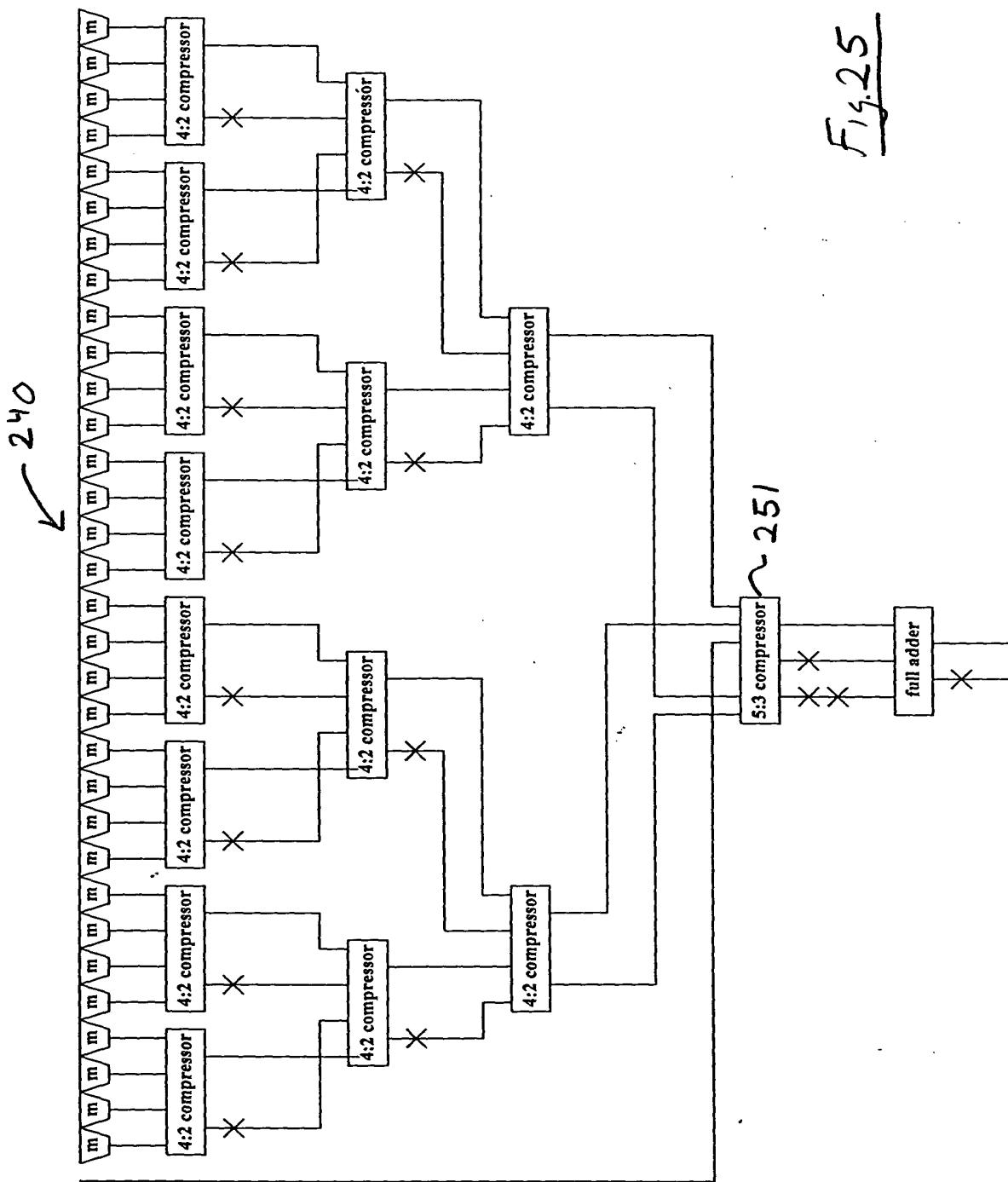
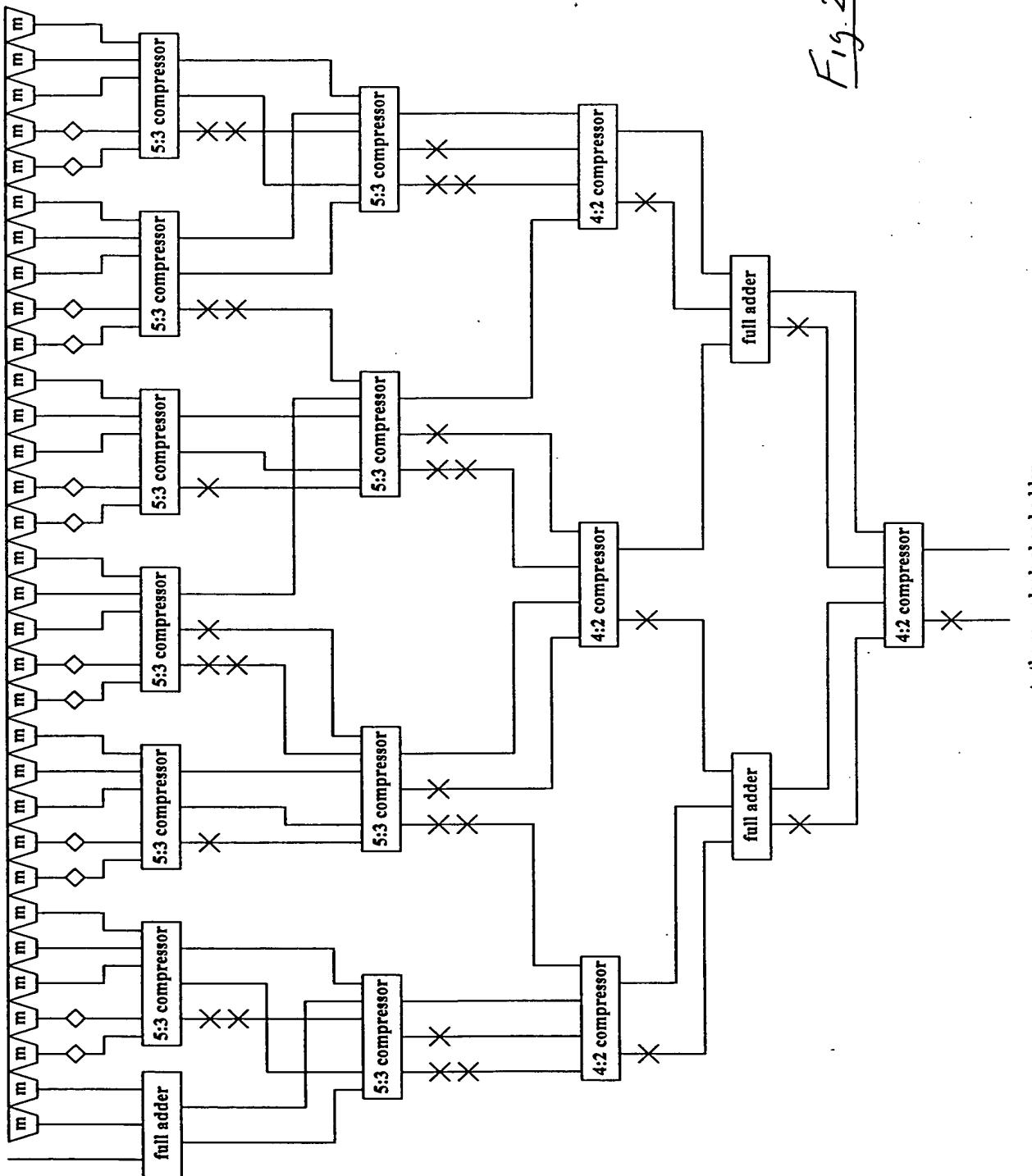
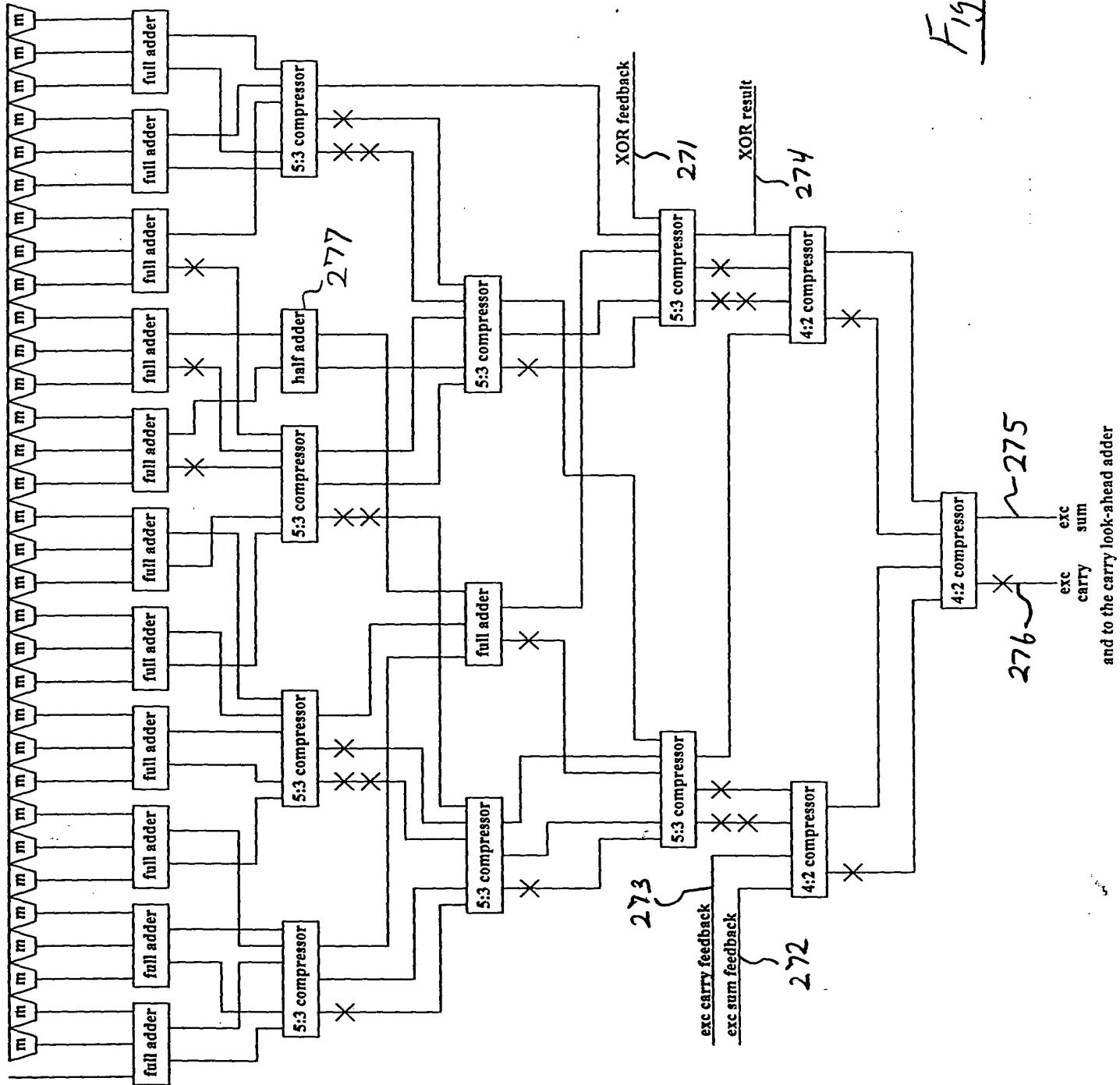


Fig. 26



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Fig. 27



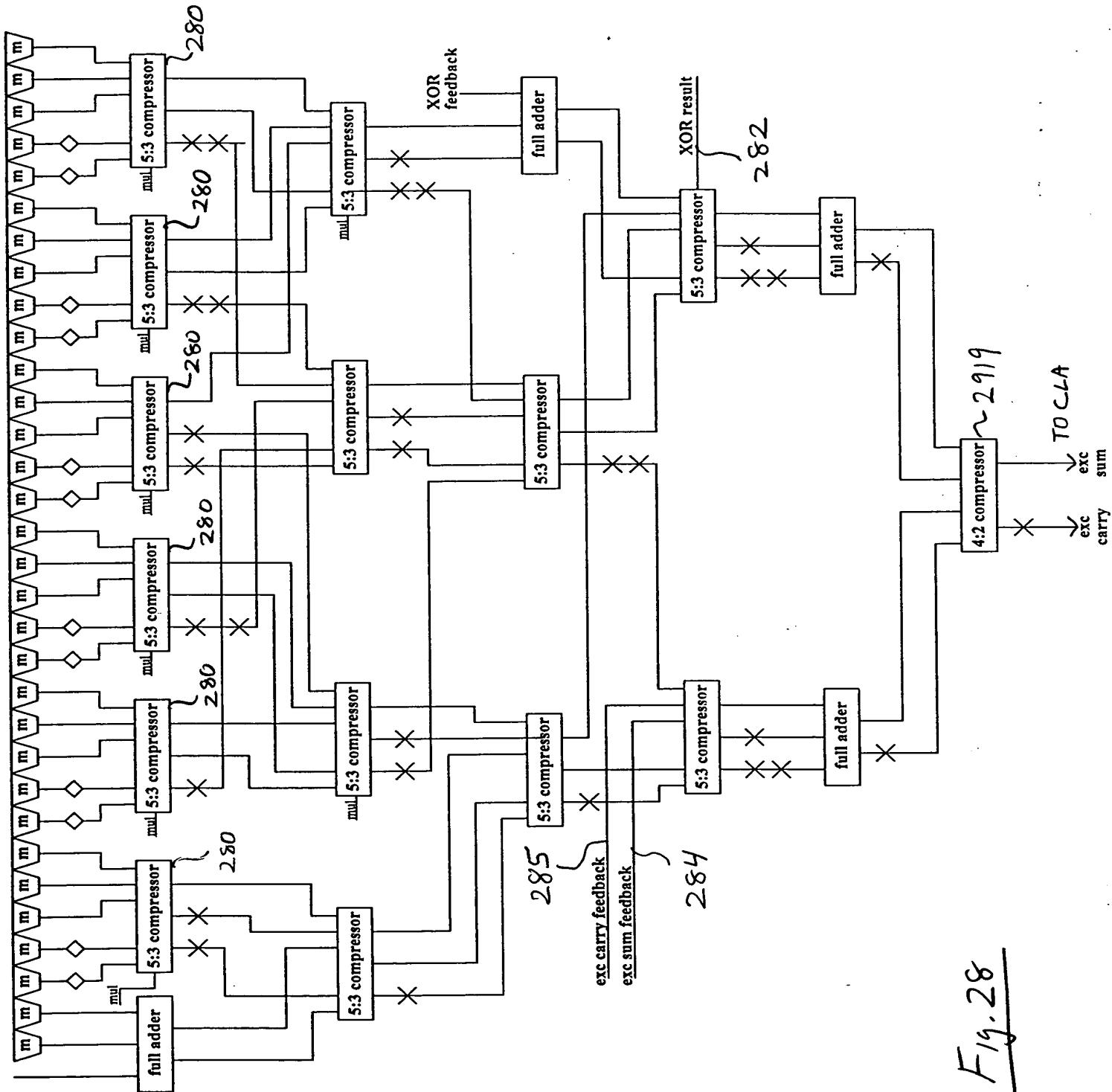


Fig. 28

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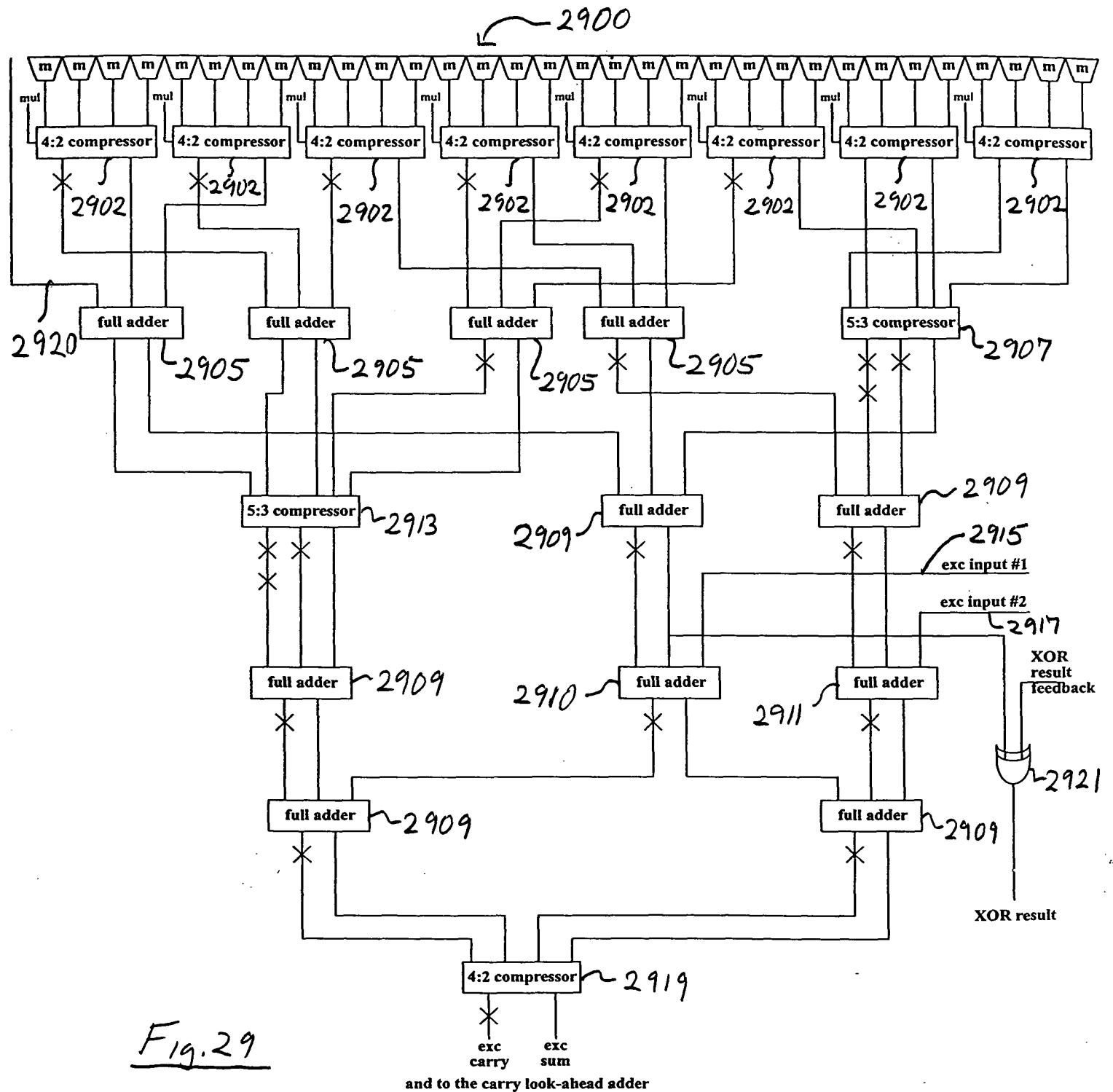


Fig. 29

and to the carry look-ahead adder

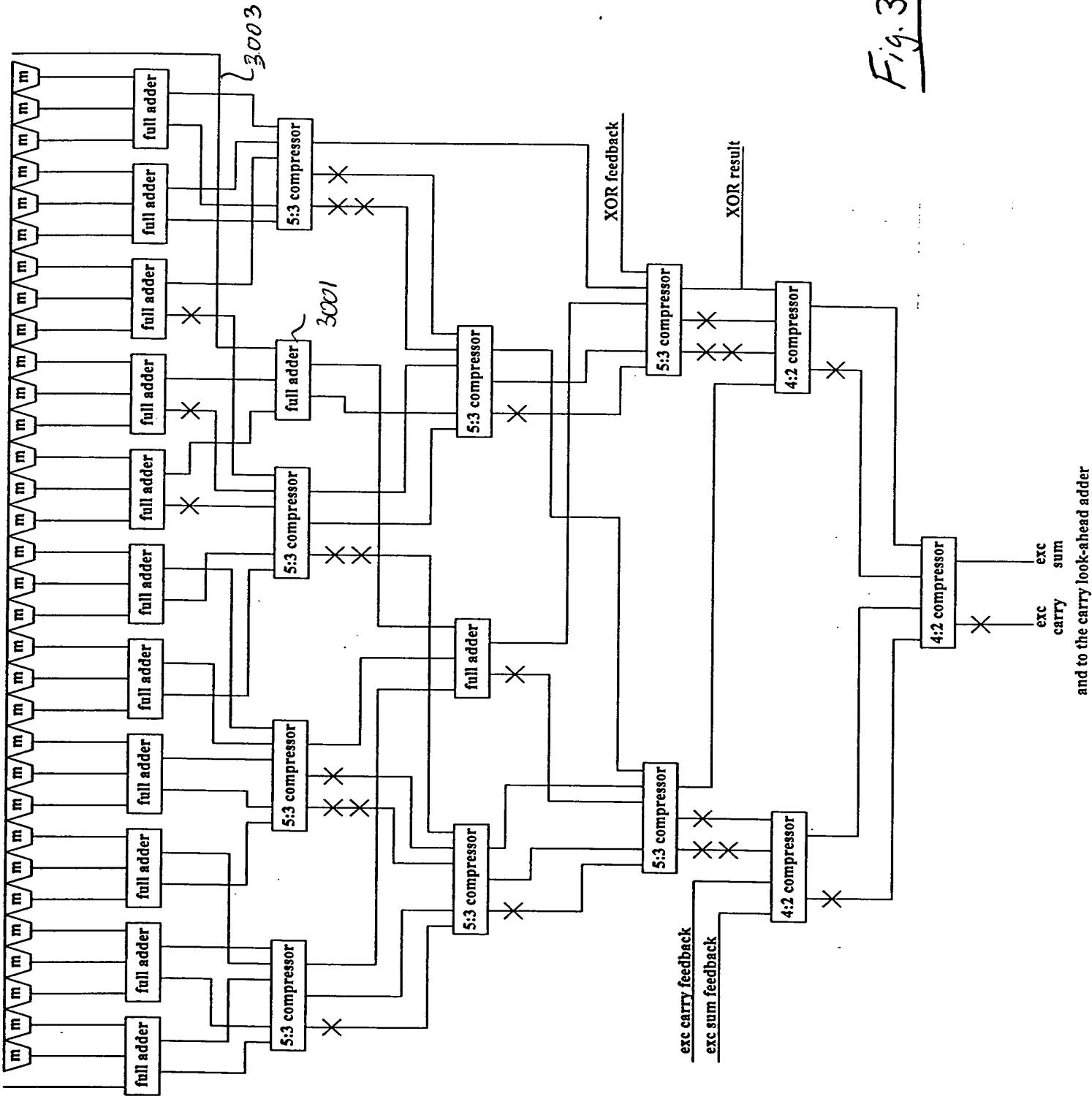


Fig. 30

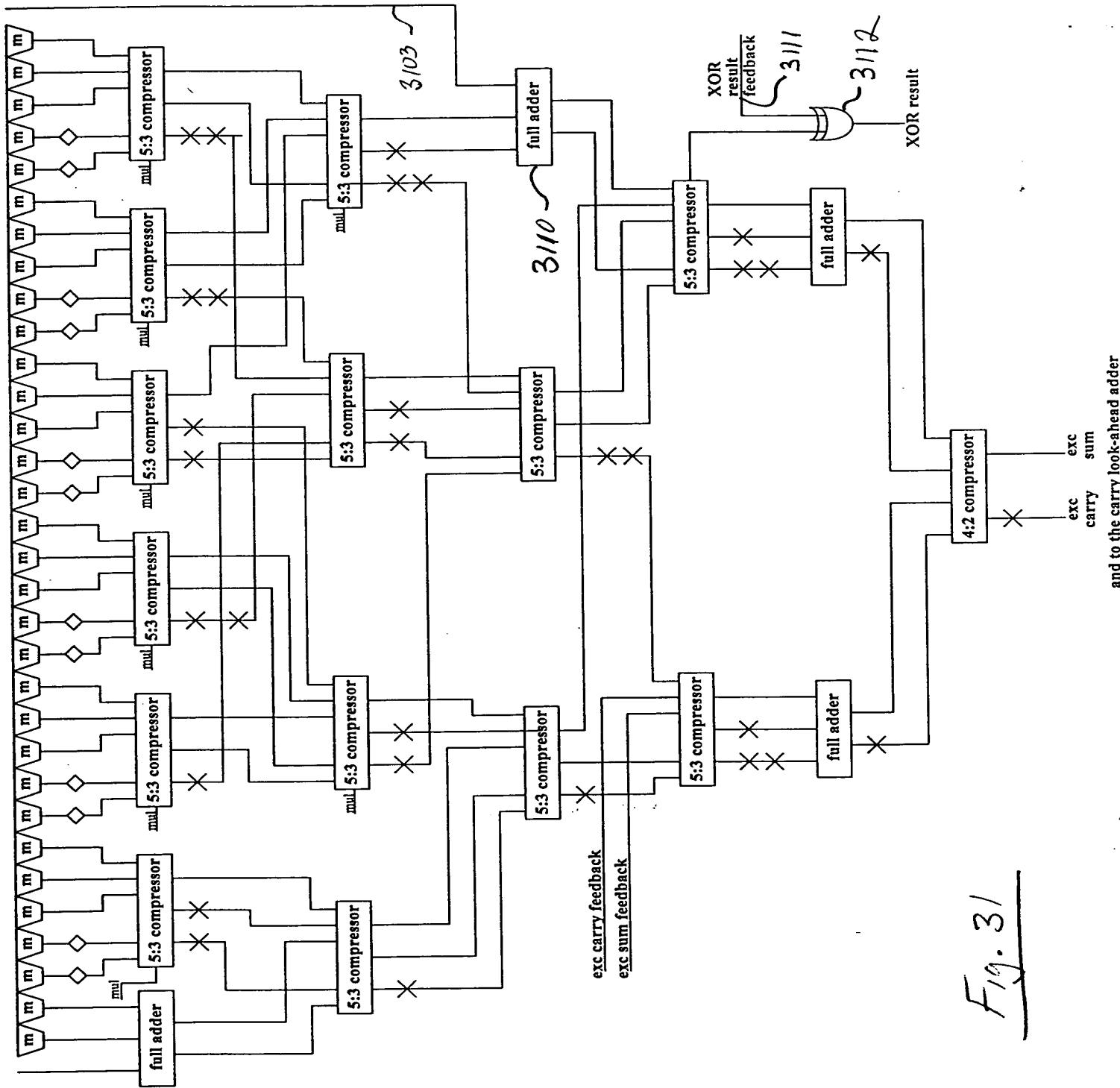


Fig. 31

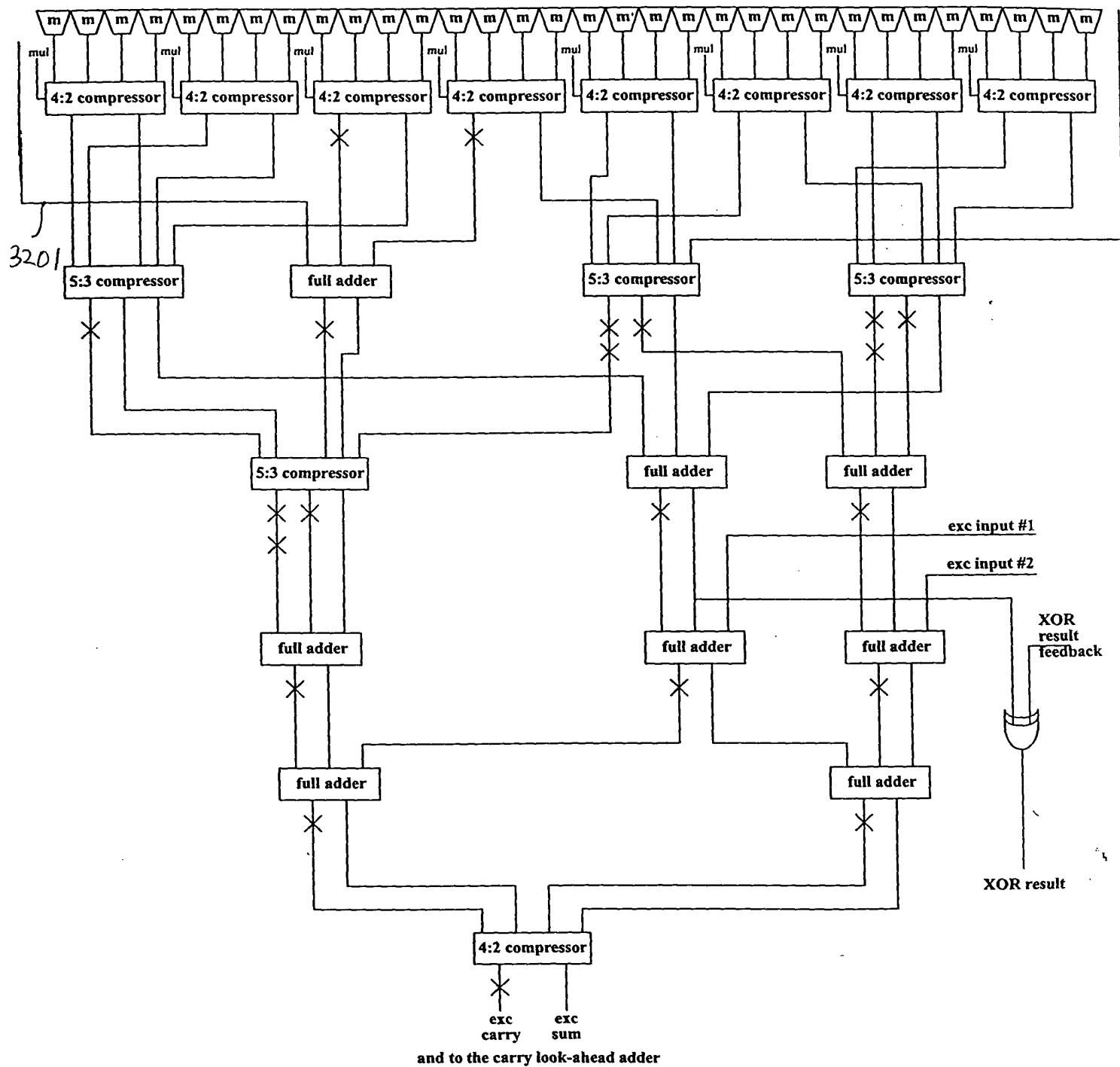


Fig. 32